TTC upgrade system
Production Readiness Review

February 2007

- System overview
- Optical Tx and Rx modules
- RF2TTC module
- Fanout
- TTC Crate
- Full system
- Documentation
- AOB

TTC RD12 [overview]

[1 + 1spare]

CMS

[2 + 1spare]

[1 + 1spare]

ALICE

LHCb

ATLAS

Magnetic field:	<100gauss
Radiations:	
Total dose:	1.4 rad/10yrs
Ch Hadrons >20MeV fluency:	1.5 10^6/10yrs/cm^{-2}
Neutrons>20MeV:	3.1 10^6/10yrs/cm^{-2}

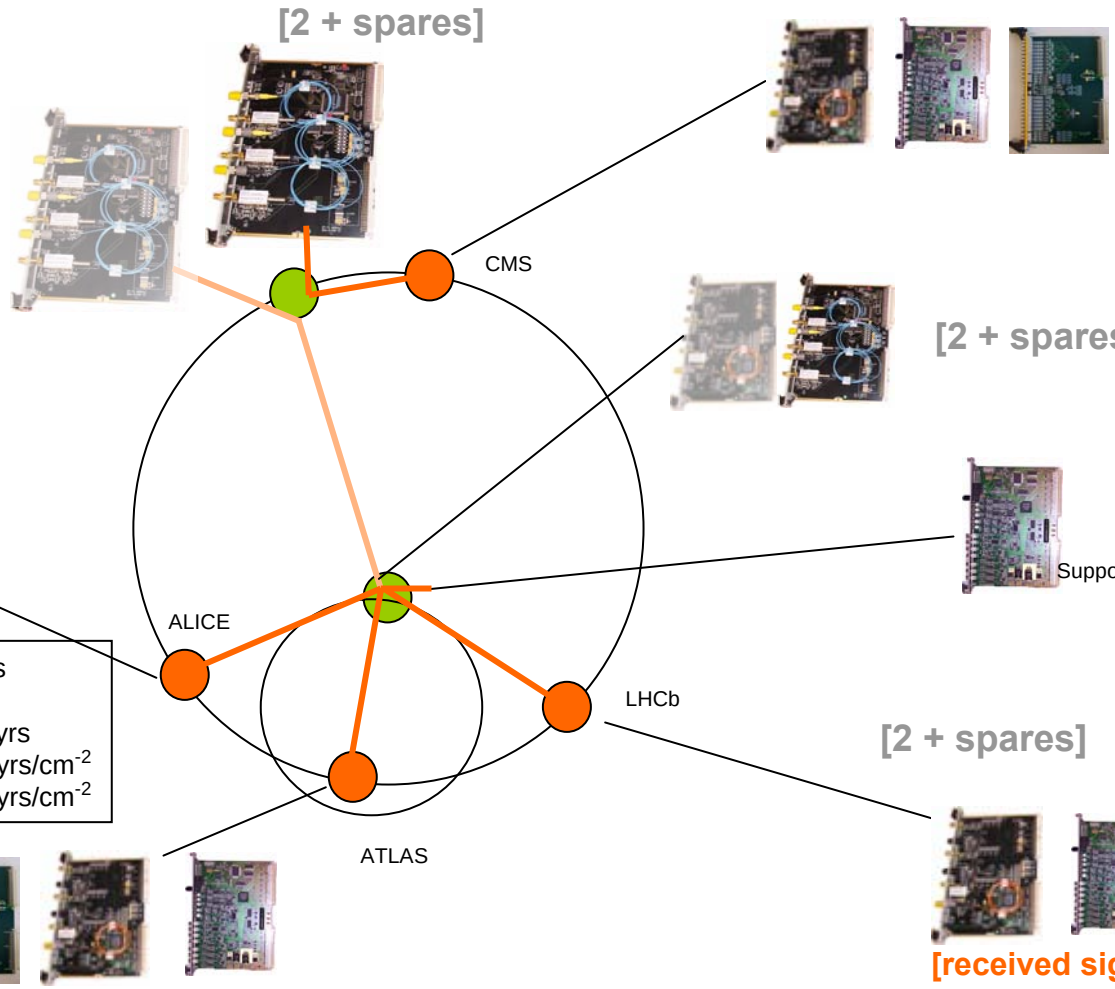
[1 + 1spare]

[received signals]
[BC1 + Orb1]
OR
[BC2 + Orb2]

[1 + 1spare]

Status mid 2004

TTC UPGRADE [overview]



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- System overview
- Optical Tx and Rx modules
  - Overview
  - Performances
  - AB/RF commitment
  - Optical budget and fibre routing
  - Schedules
  - Quantities & price estimation
- RF2TTC module
- Fanout
- TTC Crate
- Full system
- Documentation
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OPTICAL TX & RX [overview]

- Transmit 40MHz, 5ns orbit pulse (and 400MHz)
- Performances (in term of jitter or phase noise) following AB/RF requirements
- Compatible with the standard LHC VME crates and with the custom crates of the AB/RF
- Components and firmware following the AB/RF guidelines
- Monitoring of the laser optical power and of the receiver signal

OPTICAL RX [VME control & monitoring]

- Rx control:
  - Threshold adjustment (according to optical power and signal type)
  - Routines described to detect the signal type and adjust the threshold accordingly
- Rx monitoring:
  - Received frequency (few kHz resolution)
  - This frequency will have to be published on DIP for support purpose

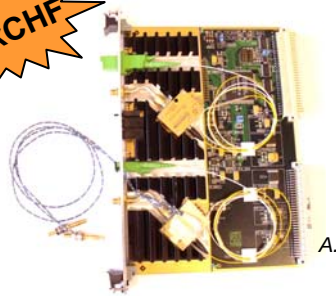
OPTICAL TX & RX [overview]

ANALOGUE SET

- Designed for RF transmission (sinewave)
- Phase noise <5ps (pk-pk!).
- 2 Optical links per module
- Optical power budget 5-10dB

11kCHF/link

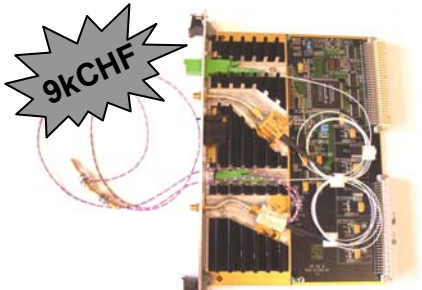
13kCHF



A. Monera, PH/ESS

RF_Tx_A
EDMS Ref: EDA-01331

9kCHF



A. Monera, PH/ESS

RF_Rx_A
EDMS Ref: EDA-01332

DIGITAL SET

- 40MHz & 5ns pulses transmission
- Jitter <30ps rms
- 3 Optical links per module
- Optical power Budget 25dB
- Various Tx and Rx can be installed

2kCHF/link

3.5kCHF

RF_Tx_D
EDMS Ref: EDA-01380
A. Monera, PH/ESS

OCP STX03-300MHz
350 $

or

OCP STX24-1.5GHz
600 $

or

Photon PT5343-300MHz
250 $ - Obsolete

2.5kCHF

RF_Tx_D
EDMS Ref: EDA-01382 *A. Monera, PH/ESS*

OCP SRX03-300MHz
200 $

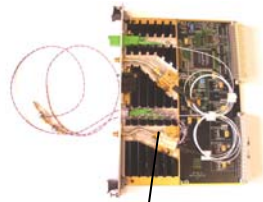
OCP SRX24-1.5GHz
300 $

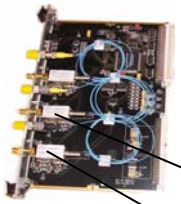
Truelight TRR-1B43-00-150MHz
8$

OPTICAL TX & RX [performances]

- The acceptance tests of the digital Tx and Rx were done in collaboration with AB/RF end of November
- The following parameters were measured:
  - Skew jitter
  - Cycle2cycle jitter
  - Period jitter over 100us
  - Rising edge of the recovered signal
  - Calculation of the ‘real’ skew jitter introduced by the link itself
- Their performances were compared to the analogue version
- All the types of signals to be transmitted were tested
  - 400MHz
  - 40MHz
  - 5ns 11kHz pulse
- The test setup was using the orbit and clock generator (VTU) which will be the source of our signals
- This setup was then used to test the full system
- All the presented results can be found on the system test report

OPTICAL TX & RX [tested configurations]

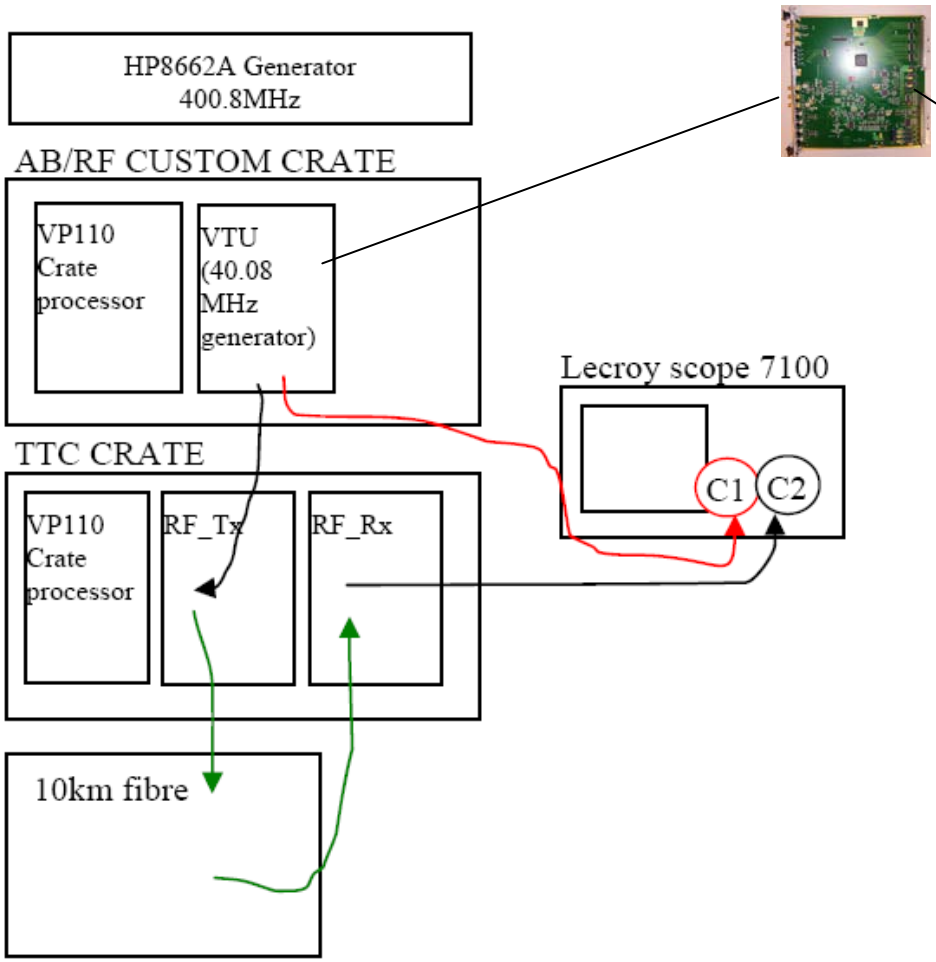


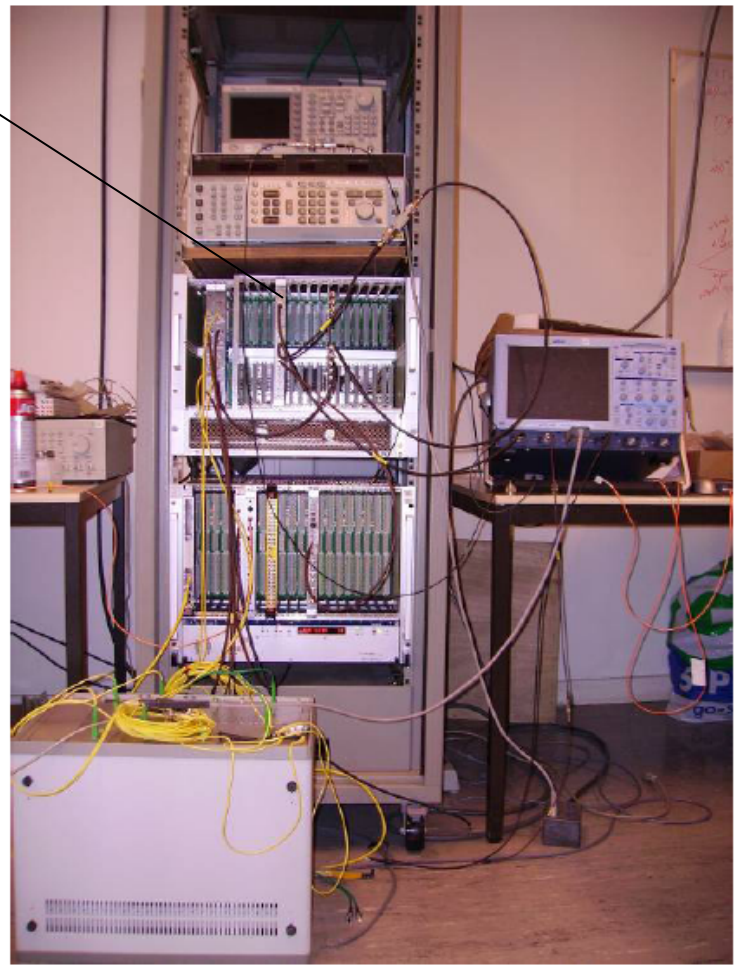


TX \ RX	OCP03-SRX	OCP24-SRX	TRR	LBL3 - Rx
OCP03-STX	40MHz	40MHz	40MHz, Pulse	-
OCP24-STX	40MHz	40MHz, 400MHz	40MHz	-
LBL3 - Tx	-	-	-	40MHz, 400MHz

OPTICAL TX & RX [40MHz]

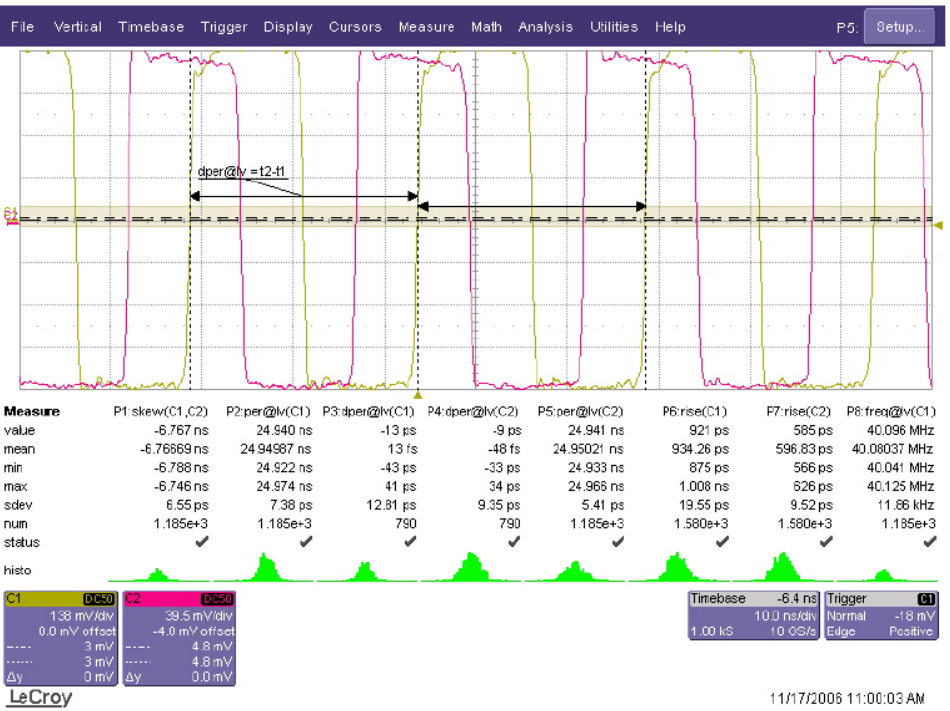
- Test Setup



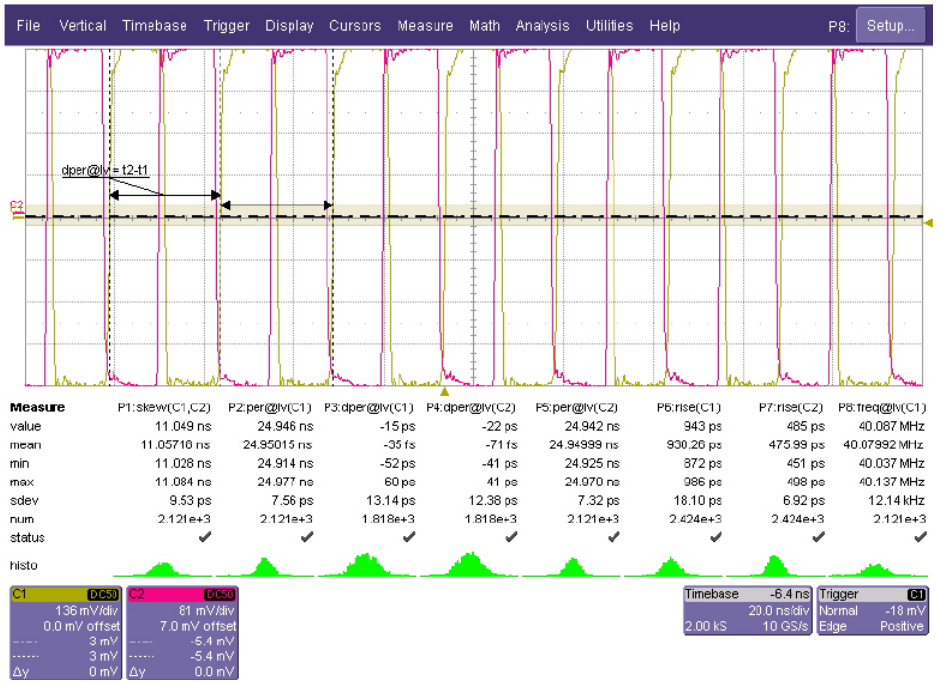


OPTICAL TX & RX [40MHz]

- Signal shapes


File Vertical Timebase Trigger Display Cursors Measure Math Analysis Utilities Help
P5: Setup...
dper@lv = t2-t1
Measure P1:skew(C1,C2) P2:per@lv(C1) P3:dper@lv(C1) P4:dper@lv(C2) P5:per@lv(C2) P6:rise(C1) P7:rise(C2) P8:freq@lv(C1)
value -6.767 ns 24.940 ns -13 ps -9 ps 24.941 ns 921 ps 585 ps 40.096 MHz
mean -6.76869 ns 24.94987 ns 13 fs -48 fs 24.95021 ns 934.26 ps 596.83 ps 40.08037 MHz
min -6.788 ns 24.922 ns -43 ps -33 ps 24.933 ns 875 ps 566 ps 40.041 MHz
max -6.746 ns 24.974 ns 41 ps 34 ps 24.966 ns 1.008 ns 626 ps 40.125 MHz
sdev 6.55 ps 7.38 ps 12.81 ps 9.35 ps 5.41 ps 19.55 ps 9.52 ps 11.86 kHz
num 1.185e+3 1.185e+3 790 790 1.185e+3 1.580e+3 1.580e+3 1.185e+3
status
histo
C1 DC50 138 mV/div 0.0 mV offset 3 mV 3 mV Δy 0 mV
C2 DC50 39.5 mV/div -4.0 mV offset 4.8 mV 4.8 mV Δy 0.0 mV
Timebase -6.4 ns 10.0 ns/div 1.00 kS 10 GS/s
Trigger C1 Normal -18 mV Edge Positive
LeCroy
11/17/2006 11:00:03 AM

Analog 40MHz versus VTU source


File Vertical Timebase Trigger Display Cursors Measure Math Analysis Utilities Help
P8: Setup...
dper@lv = t2-t1
Measure P1:skew(C1,C2) P2:per@lv(C1) P3:dper@lv(C1) P4:dper@lv(C2) P5:per@lv(C2) P6:rise(C1) P7:rise(C2) P8:freq@lv(C1)
value 11.049 ns 24.946 ns -15 ps -22 ps 24.942 ns 943 ps 485 ps 40.087 MHz
mean 11.05716 ns 24.95015 ns -35 fs -71 fs 24.94999 ns 930.26 ps 475.99 ps 40.07992 MHz
min 11.028 ns 24.914 ns -52 ps -41 ps 24.925 ns 872 ps 451 ps 40.037 MHz
max 11.084 ns 24.977 ns 60 ps 41 ps 24.970 ns 986 ps 498 ps 40.137 MHz
sdev 9.53 ps 7.56 ps 13.14 ps 12.38 ps 7.32 ps 18.10 ps 6.92 ps 12.14 kHz
num 2.121e+3 2.121e+3 1.818e+3 1.818e+3 2.121e+3 2.424e+3 2.424e+3 2.121e+3
status
histo
C1 DC50 136 mV/div 0.0 mV offset 3 mV 3 mV Δy 0 mV
C2 DC50 81 mV/div 7.0 mV offset -5.4 mV -5.4 mV Δy 0.0 mV
Timebase -6.4 ns 20.0 ns/div 2.00 kS 10 GS/s
Trigger C1 Normal -18 mV Edge Positive

OCP03-STX & TRR link versus VTU source

OPTICAL TX & RX [40MHz]

- Skew jitter (Rx output versus VTU output)
  - Standard deviation

TX \ RX	OCP03-SRX	OCP24-SRX	**TRR**	LBL3
OCP03-STX	9.55ps rms	8.78ps rms	**9.28ps rms**	-
OCP24-STX	9.13ps rms	8.92ps rms	9.96ps rms	-
LBL3- Tx	-	-	-	6.75ps rms

  - Peak to peak

TX \ RX	OCP03-SRX	OCP24-SRX	**TRR**	LBL3
OCP03-STX	77ps pkpk	64ps pkpk	**71ps pkpk**	-
OCP24-STX	70 ps pkpk	71ps pkpk	88ps pkpk	-
LBL3- Tx	-	-	-	90ps pkpk*

*Relatively high value which can be explained by the quantity of samples considered for this measurement: 100ks instead of 30ks for the other configurations.

OPTICAL TX & RX [40MHz]

- Cycle-to-cycle jitter
  - Standard deviation *(source reference=13.14ps rms)*

TX \ RX	OCP03-SRX	OCP24-SRX	**TRR**	LBL3
OCP03-STX	11ps rms	10.5ps rms	**12.54ps rms**	-
OCP24-STX	10.97ps rms	10.63ps rms	14.6ps rms	-
LBL3- Tx	-	-	-	9.83ps rms

  - Peak to peak *(source reference=128ps pkpk)*

TX \ RX	OCP03-SRX	OCP24-SRX	**TRR**	LBL3
OCP03-STX	109 ps pkpk	90ps pkpk	**104ps pkpk**	-
OCP24-STX	93 ps pkpk	94ps pkpk	130 ps pkpk	-
LBL3- Tx	-	-	-	180ps pkpk

OPTICAL TX & RX [40MHz]

- Period jitter over 100us (to take the transmission delay into account (50us))
  - Standard deviation *(source reference=7.5ps rms)*

TX \ RX	OCP03-SRX	OCP24-SRX	**TRR**	LBL3
OCP03-STX	6.42ps rms	6.07ps rms	**7.29ps rms**	-
OCP24-STX	6.47ps rms	6.15ps rms	8.50ps rms	-
LBL3- Tx	-	-	-	5.68ps rms

  - Peak to peak *(source reference=68ps pkpp)*

TX \ RX	OCP03-SRX	OCP24-SRX	**TRR**	LBL3
OCP03-STX	64ps pkpk	51ps pkpk	**62ps pkpk**	-
OCP24-STX	53ps pkpk	57ps pkpk	73ps pkpk	-
LBL3- Tx	-	-	-	116ps pkpk

OPTICAL TX & RX [40MHz]

- Rising edge
  - Mean value *(source reference = 935ps)*

TX \ RX	OCP03-SRX	OCP24-SRX	**TRR**	LBL3
OCP03-STX	474ps	470ps	**475ps**	-
OCP24-STX	473ps	469ps	475ps	-
LBL3- Tx	-	-	-	597ps

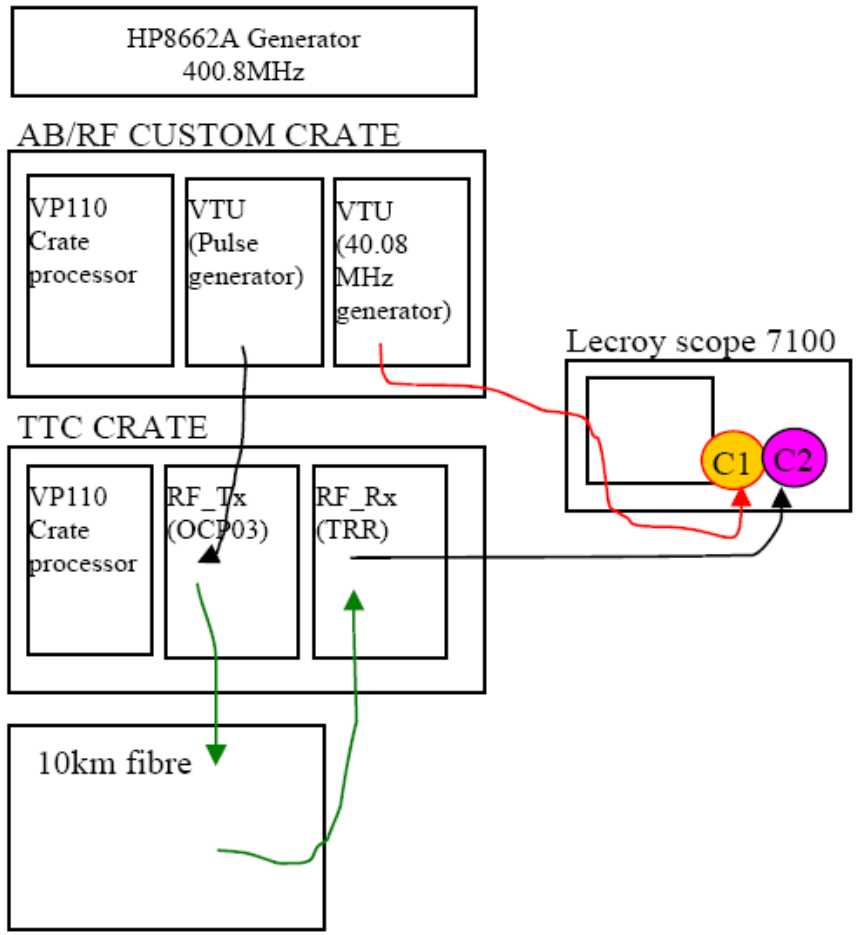
- Summary

	OCP03-TRR	SCOPE JNF	CORRECTED MEAS
Skew	9 ps rms**	4.5ps rms*	7.8ps rms
Cycle2cycle	12 ps rms	7.5ps rms*	9.4ps rms
Period	7ps rms	4.5ps rms*	5.4ps rms

*These values should be quadratically removed from the previous measurement
**Corrected value of the skew jitter, removing the period jitter, is 5.5ps rms

OPTICAL TX & RX [5ns Pulse]

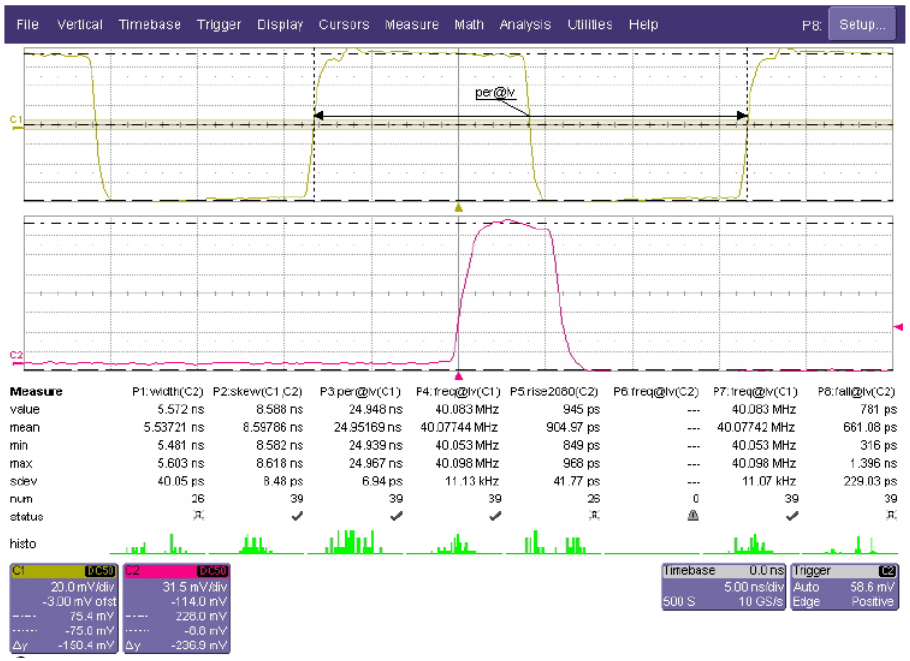
- Test Setup
  - 5ns pulse synchronised to 40.08Mhz
  - Only OCP03-TRR tested in this configuration



OPTICAL TX & RX [5ns Pulse]

- Results

	Width	Skew jitter (C1, C2)	Rising edge	Falling Edge
Mean of the reference (VTU pulse)	5.5ns	8.5ps	905ps	661ps
Mean value	5.66ns		319ps	339ps
Standard Dev	13.9ps rms	24.9ps rms	5ps rms	5.96ps rms
pkpk	79ps pkpk	136 ps pkpk	30ps pkpk	30ps pkpk


File Vertical Timebase Trigger Display Cursors Measure Math Analysis Utilities Help
P8: Setup...
per@lv
C1
C2
Measure P1:width(C2) P2:skew(C1,C2) P3:per@lv(C1) P4:freq@lv(C1) P5:rise2080(C2) P6:freq@lv(C2) P7:freq@lv(C1) P8:fall@lv(C2)
value 5.572 ns 8.588 ns 24.948 ns 40.083 MHz 945 ps --- 40.083 MHz 781 ps
mean 5.53721 ns 8.59786 ns 24.95169 ns 40.07744 MHz 904.97 ps --- 40.07742 MHz 661.08 ps
min 5.481 ns 8.582 ns 24.939 ns 40.053 MHz 849 ps --- 40.053 MHz 316 ps
max 5.603 ns 8.618 ns 24.967 ns 40.098 MHz 968 ps --- 40.098 MHz 1.396 ns
sdev 40.05 ps 8.48 ps 6.94 ps 11.13 kHz 41.77 ps --- 11.07 kHz 229.03 ps
num 26 39 39 39 26 0 39 39
status
histo
C1 DC50 20.0 mV/div -3.00 mV ofst 75.4 mV -75.0 mV Δy -150.4 mV
C2 DC50 31.5 mV/div -114.0 mV 228.0 mV -8.0 mV Δy -236.9 mV
Timebase 0.0 ns 5.00 ns/div 500 S 10 GS/s
Trigger Auto 58.6 mV Edge Positive

VTU 40.08MHz and 5ns Pulse reference

File Vertical Timebase Trigger Display Cursors Measure Math Analysis Utilities Help
C2 Setup...
per@lv
C1
C2
Measure P1:width(C2) P2:skew(C1,C2) P3:per@lv(C1) P4:freq@lv(C1) P5:rise2080(C2) P6:freq@lv(C2) P7:freq@lv(C1) P8:fall@lv(C2)
value 5.653 ns 4.352 ns 24.918 ns 40.131 MHz 324 ps --- 40.131 MHz 333 ps
mean 5.66435 ns 4.34706 ns 24.95032 ns 0 GHz 319.35 ps --- 0 GHz 336.66 ps
min 5.620 ns 4.280 ns 24.855 ns 0 THz 303 ps --- 0 THz 325 ps
max 5.699 ns 4.416 ns 25.019 ns 0 THz 335 ps --- 0 THz 357 ps
sdev 13.90 ps 24.83 ps 29.25 ps 0 GHz 5.19 ps --- 0 GHz 5.96 ps
num 242 242 242 242 242 0 242 242
status
histo
C1 DC50 100 mV/div -3.0 mV offset 385 mV -387 mV Δy -752 mV
C2 DC50 102 mV/div -410.0 mV 779 mV 12 mV Δy -767 mV
Timebase -2.2 ns 5.00 ns/div 500 S 10 GS/s
Trigger Auto 125 mV Edge Positive

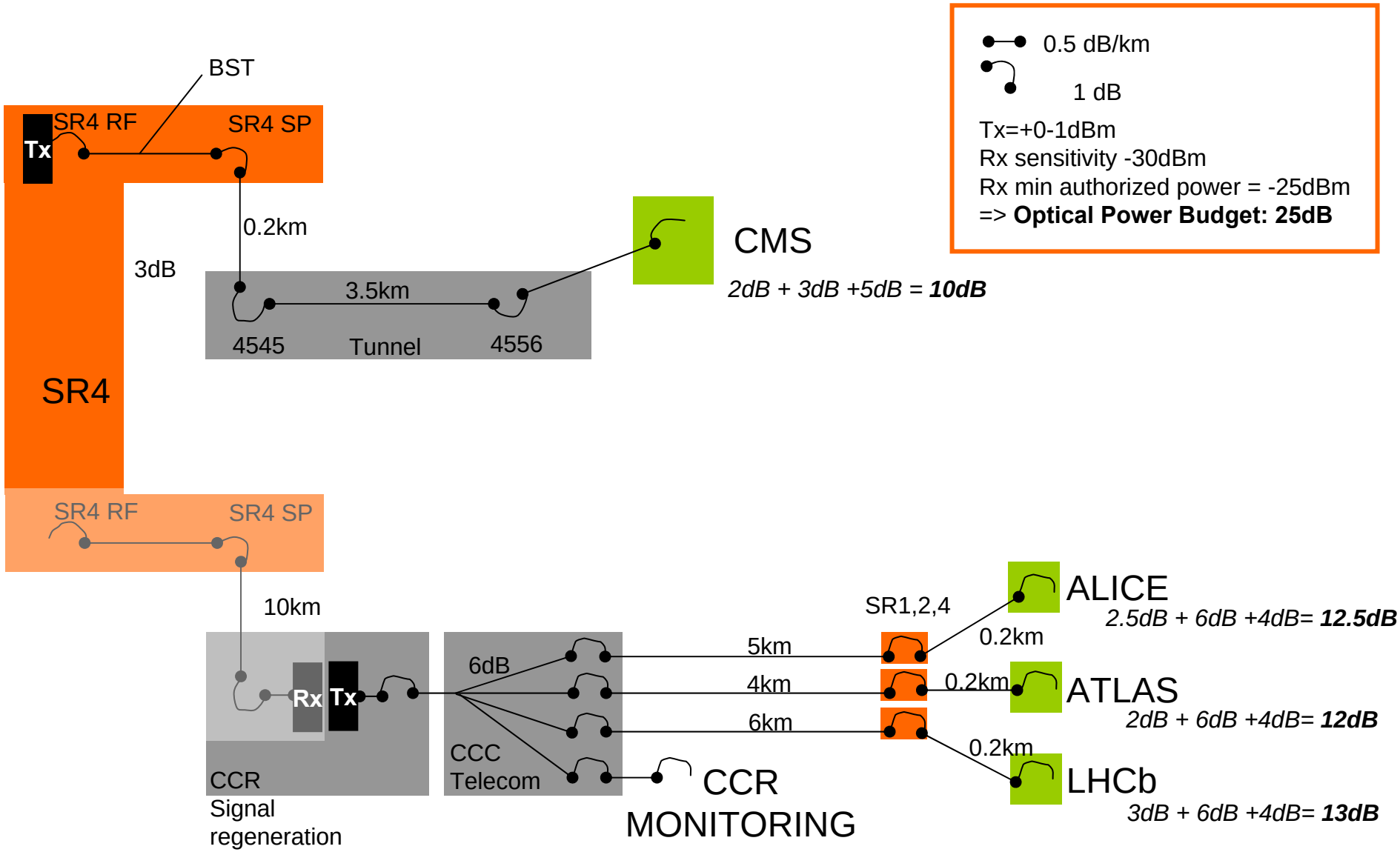
Transmitted Pulse versus reference clock

AB/RF CONCLUSIONS & COMMITMENT

- "The prototype v1 RF_Rx_D and RF_Tx_D have been tested in November with the LHC signals: 5 ns,1 Vpk pulses (Orbit), 40 MHz square and sine wave (Bunch Clock) and 400 MHz (RF). ***The results are fully satisfactory***. See report by S. Baron.
  As the designer in the PH department is leaving, ***AB/RF/FB takes responsibility for the future of these modules***:
  We will launch a version 2 in January 2007. This version 2 has only minor differences with version 1.
  In parallel we will start ordering key components such as the optical TX and RX.
  By April 2007 we launch series production for installation in summer 2007.
  The transmission can then be commissioned in Sept 2007. (If this schedule is not satisfactory it can be discussed).
  PH department should take care of the order and installation of the modules used by the experiments except at the sending end SR4 and in the RF racks in CCR. The modules used by the experiments will be paid by them, including spares stored locally.
  During LHC operation AB/RF/FB will be responsible for maintenance and piquet service on these transmissions. The modules are equipped with diagnostics and PH will make these diagnostics "readable" by AB/OP and AB/RF. (As the OS in the VME CPU is different in AB and PH, some "driver" must be developed by PH. To be discussed).
  The modules (eda-01380 and eda-01382) are fully documented in edms so that for future orders the user will contact TS/DEM directly. "

  P. Baudrenghien, December 06

FIBRE ROUTING



SCHEDULES

- Routing
  - Patching of option1:
    - February = NOW
  - Measurement of the optical losses:
    - March
  - *Tests can thus be done with prototypes Tx and Rx on these fibres, but probably without the AB/RF group*

- RF modules & signals:
  - According to AB/RF commitment
  - Version 2: schematics and layout being modified now
    - Request from CMS (Design Review, May06) to separate fibres from cables is rejected for practical reasons
  - Modules production: April 07
  - Installation: Summer 07
  - Signals transmission: September 07
  - *"If this schedule is not satisfactory it can be discussed" => not anymore!*

QUANTITIES & PRICE

- To be discussed

	Used	Hot Spares	Cold Spares	Unit price	Total quantities	Total Price kCHF
Tx	4*	2	2	3.5 kCHF	8	28 kCHF***
Rx	10**	5	5	2.5 kCHF	20	50 kCHF
						78 kCHF

* 2 Tx in CCR for ALICE, ATLAS, LHCb & Support, 2 in SR4 for CMS

** 2 Rx per experiment, + 2 for the CCR-monitoring

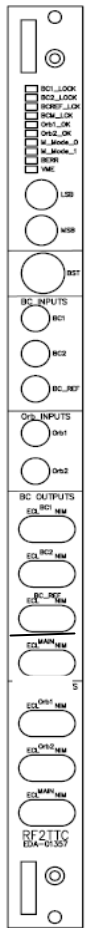
*** To be discussed with AB/RF

Price per experiment: 19.5kCHF

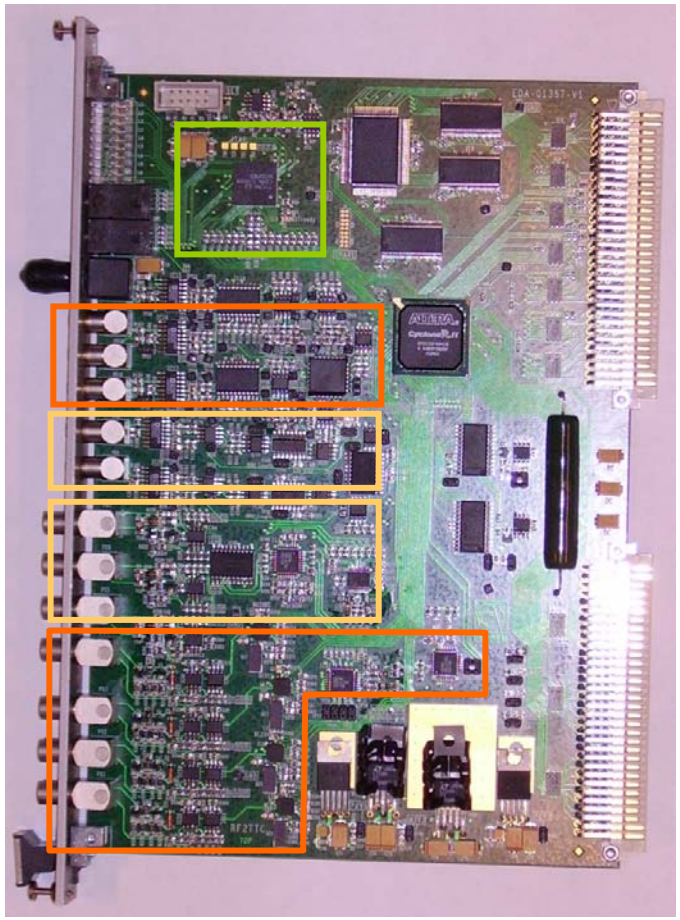
- System overview
- Optical Tx and Rx modules
- RF2TTC module
  - Overview
  - Performances
  - Functions
  - Work with the first users
  - Foreseen changes from V2 to V3
  - Quantities & price estimation
  - Software integration
  - Schedules
- Fanout
- TTC Crate
- Full system
- Documentation
- AOB

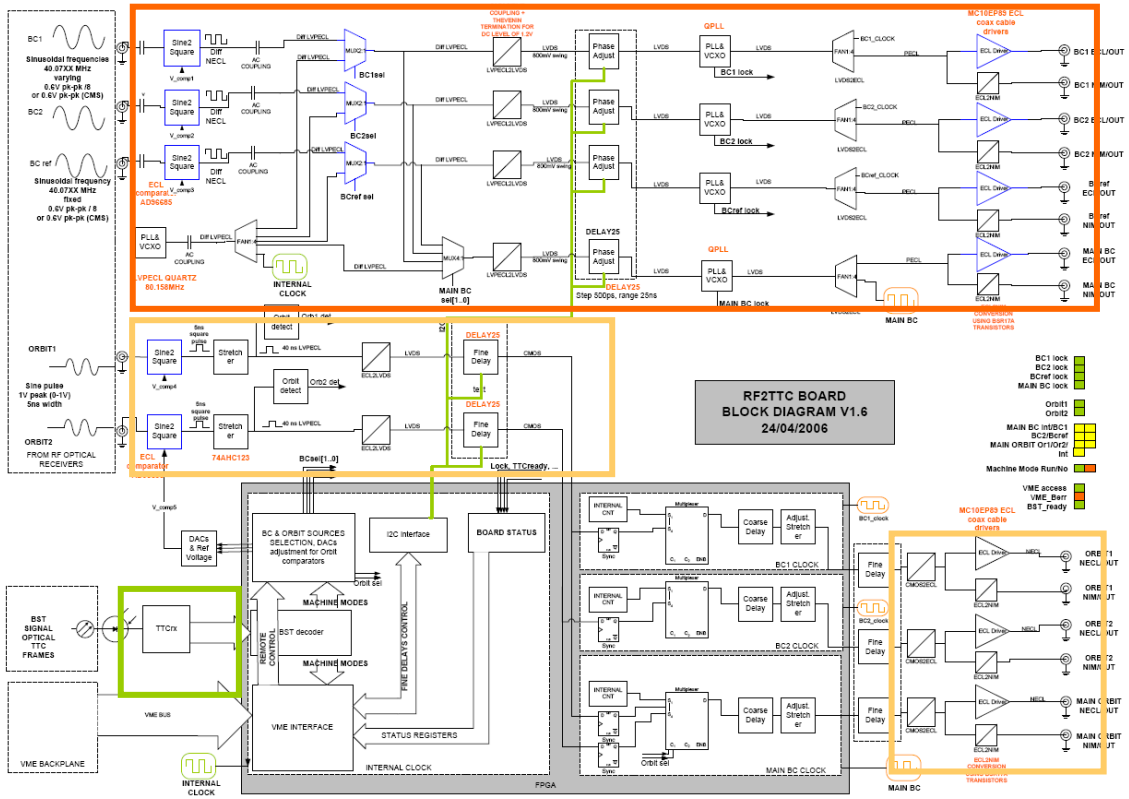
RF2TTC [overview]

- RF2TTC
  - RF to TTC VMEbus Interface Card
  - Interface card between the optical receiver modules and the TTCC electronics within the experiments.
  - Treated timing signals
    - three 40.078MHz Bunch Clocks (BC1, BC2 and BCref)
    - two orbit signals (Orb1 and Orb2) necessary to drive the 2 beam lines of the LHC.
  - The RF2TTC module converts them into ECL signals, and performs various adjustments on each signal before making them available for the in-detector TTC electronics.



RF2TTC [overview]





RF2TTC [review follow-up]

? - Jan asked to have an adjustable internal clock (in addition to the oscillator already installed). This could be done using a synthesizer, but will require some extra work and will induce some delays that we can not afford now. This could be implemented in the last version, if required.

ok - Jorgen suggested adding a security when the counter values are read back to avoid any transition values to be read. (ex: an intermediate register synchronised to the counter)

ok - Philippe asked to put a 10W resistor on the input of the LT1185 regulator making the -5V from the -12V. Jorgen insisted on the fact that this solution must be used if there is no big change in the current consumption of the -5 and -3.3V components. As they are only ECL components and comparators, it should be ok.

ok - Fabio insisted on the fact that DC-DC must not be used for magnetic field tolerance reasons.

x - Fabio suggested that we add some Fuses to protect the board. If possible, I will add some solid state resettable SMD fuses.

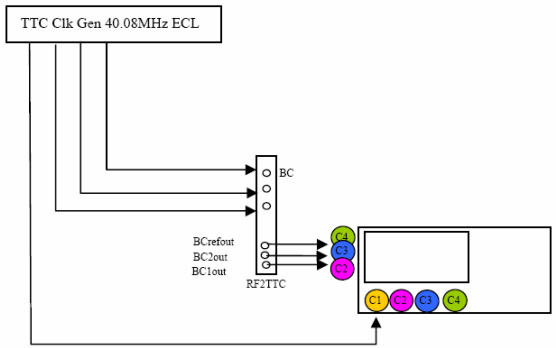
\- - Fabio asked for redundancy of the configuration registers stored in the FPGA to protect them against single event.

ok - Fabio asked, if possible, that I add a way to check the configuration of the FPGA (in case of SEU in the configuration), and that I provide an optional way to reconfigure the FPGA with the SYSreset.

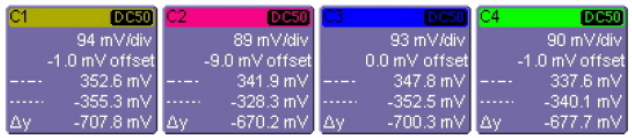
RF2TTC [performances]

- The test setup was using
  - The TTC Clock Generator
  - The orbit and clock generator (VTU) which will be the source of our signals
  - Tests of BC1_out, BC2_out, BCref_out and BCmain_out
  - Internal and external orbits
- Tested parameters
  - Bunch Clocks
    - Skew jitter
    - Cycle to cycle jitter
    - Period jitter
  - Orbit
    - Skew jitter versus synchronising clock
    - Width (standard deviation)
    - Rising edge/falling edge
- All the presented results can be found on the system test report

- Setup with the TTC Clock Generator

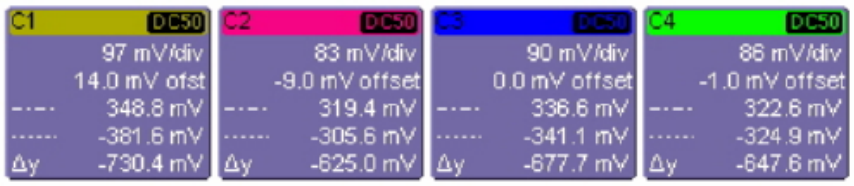


Measure	P1:skew(C1,C2)	P2:skew(C1,C3)	P3:skew(C1,C4)	P4:dper@lv(C1)	P5:dper@lv(C2)	P6:dper@lv(C3)	P7:dper@lv(C4)	P8:per@lv(C1)
value	156 ps	162 ps	256 ps	-20 ps	10 ps	5 ps	-8 ps	24.946 ns
mean	151.53 ps	166.04 ps	256.45 ps	-1 fs	-1 fs	1 fs	1 fs	24.95113 ns
min	117 ps	136 ps	227 ps	-58 ps	-54 ps	-55 ps	-50 ps	24.918 ns
max	182 ps	195 ps	287 ps	64 ps	60 ps	60 ps	57 ps	24.982 ns
sdev	8.23 ps	7.88 ps	7.87 ps	14.90 ps	14.03 ps	14.40 ps	12.68 ps	8.58 ps
num	16.024e+3	16.024e+3	16.024e+3	16.020e+3	16.020e+3	16.020e+3	16.020e+3	16.024e+3
status	✔	✔	✔	✔	✔	✔	✔	✔
histo								



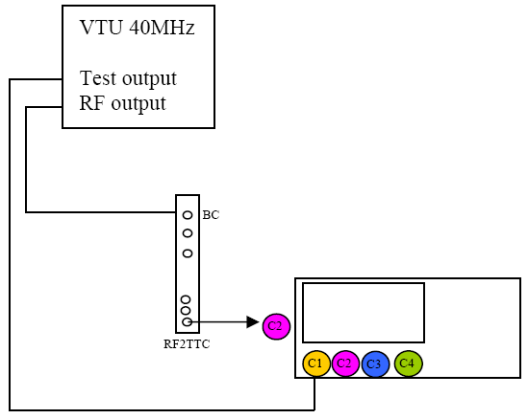
Jitter measurements of the various outputs of the TTC clock generator

	BC1	BC2	BCref	REF	BC1	BC2	BCref	REF
Measure	P1:skew(C1,C2)	P2:skew(C1,C3)	P3:skew(C1,C4)	P4:dper@lv(C1)	P5:dper@lv(C2)	P6:dper@lv(C3)	P7:dper@lv(C4)	P8:per@lv(C1)
value	-9.617 ns	-9.755 ns	-9.744 ns	8 ps	4 ps	3 ps	-8 ps	24.954 ns
mean	-9.60525 ns	-9.74468 ns	-9.76754 ns	0 fs	0 fs	0 fs	-0 fs	24.95113 ns
min	-9.670 ns	-9.819 ns	-9.833 ns	-63 ps	-32 ps	-28 ps	-27 ps	24.913 ns
max	-9.537 ns	-9.671 ns	-9.706 ns	76 ps	27 ps	27 ps	26 ps	24.992 ns
sdev	17.19 ps	16.69 ps	16.61 ps	14.64 ps	6.27 ps	6.17 ps	6.05 ps	8.45 ps
num	168.294e+3	168.294e+3	168.294e+3	168.210e+3	168.252e+3	168.252e+3	168.252e+3	168.252e+3
status	✔	✔	✔	✔	✔	✔	✔	✔
histo								



RF2TTC [Bunch Clocks – Proto1]

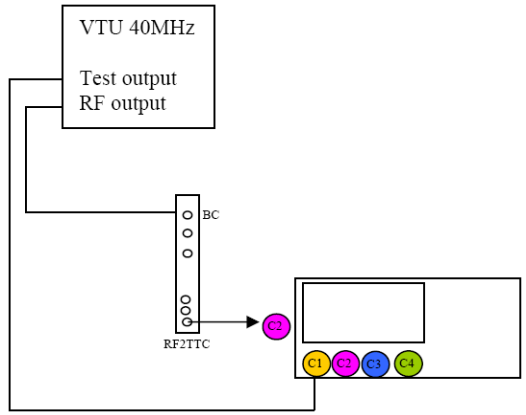
- Setup with the VTU generator
  - One output measured at a time
    - C1: Test output of the VTU, 150mV, used as a reference
    - C2: RF2TTC output, ECL, with the respective input connected to “RF output”



	Skew (std dev) ps rms	Skew (Pkpk) ps	Cy2Cy (std dev) ps rms	Cy2cy (pkpk) ps	Per (std dev) ps rms	Per (Pkpk) ps
RF output	5	45	11	110	6	55
BC1 out	13	90	6	50	4	27
BC2 out	12	75	7	50	4	30
BCref out	34	170	6	53	4	32
BCmain as BC1	14	90	6	53	4	31
BCmain as BCref	23	145	6	51	4	31

RF2TTC [Bunch Clocks - Proto2]

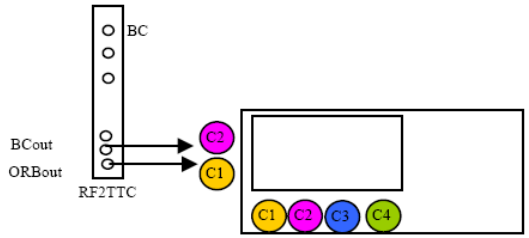
- Setup with the VTU generator
  - One output measured at a time
    - C1: Test output of the VTU, 150mV, used as a reference
    - C2: RF2TTC output, ECL, with the respective input connected to “RF output”



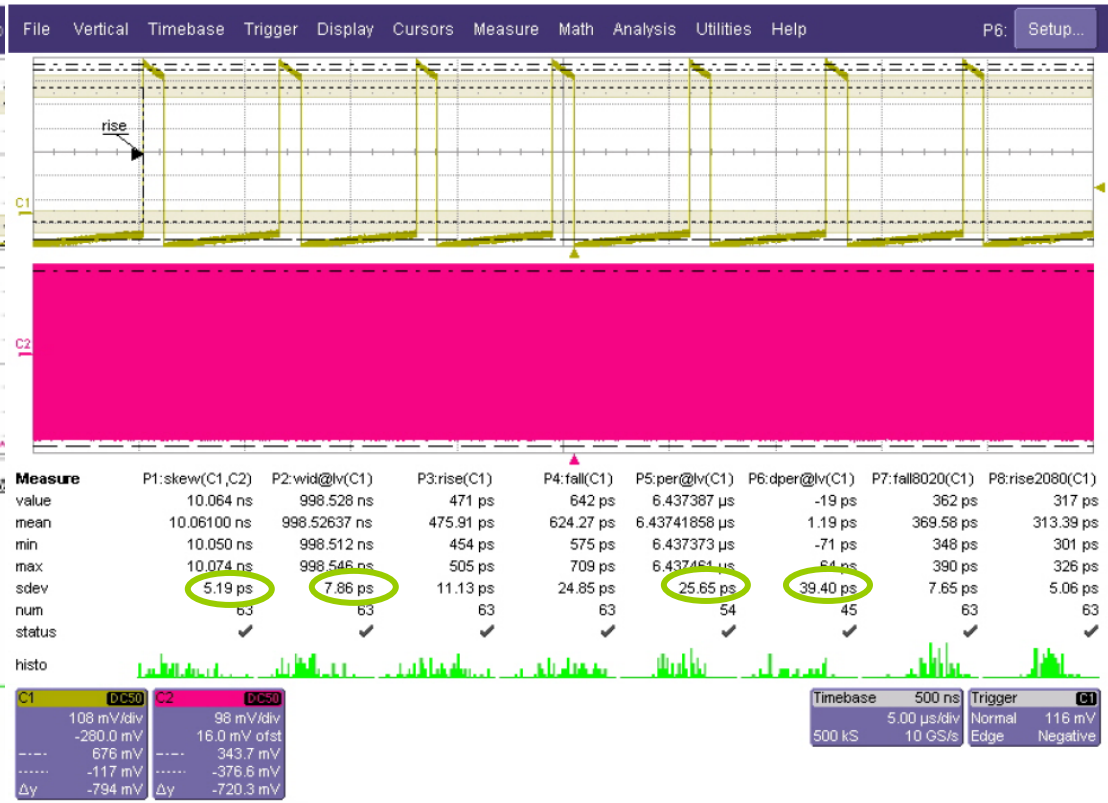
	Skew (std dev) ps rms	Skew (Pkpk) ps	Cy2Cy (std dev) ps rms	Cy2cy (pkpk) ps	Per (std dev) ps rms	Per (Pkpk) ps
RF output	4.5	42	9.9	115	5.7	65
BC1 out	11.9	102	5.9	50	3.7	31
BC2 out	16.6	112	6.1	51	3.6	30
BCref out	16.1	118	6.6	62	3.8	34
BCmain as BC1	14.9	90	6	52	3.5	30
BCmain as BCref	17.5	127	6.5	58	3.7	31

RF2TTC [Orbits]

- Internal orbit
  - Positive pulse
  - 3BC and 40BC wide pulse

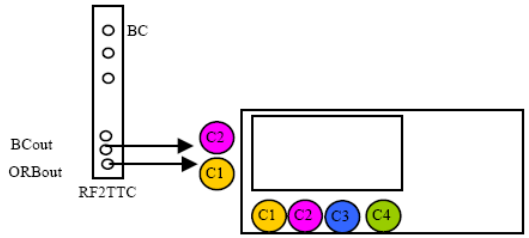


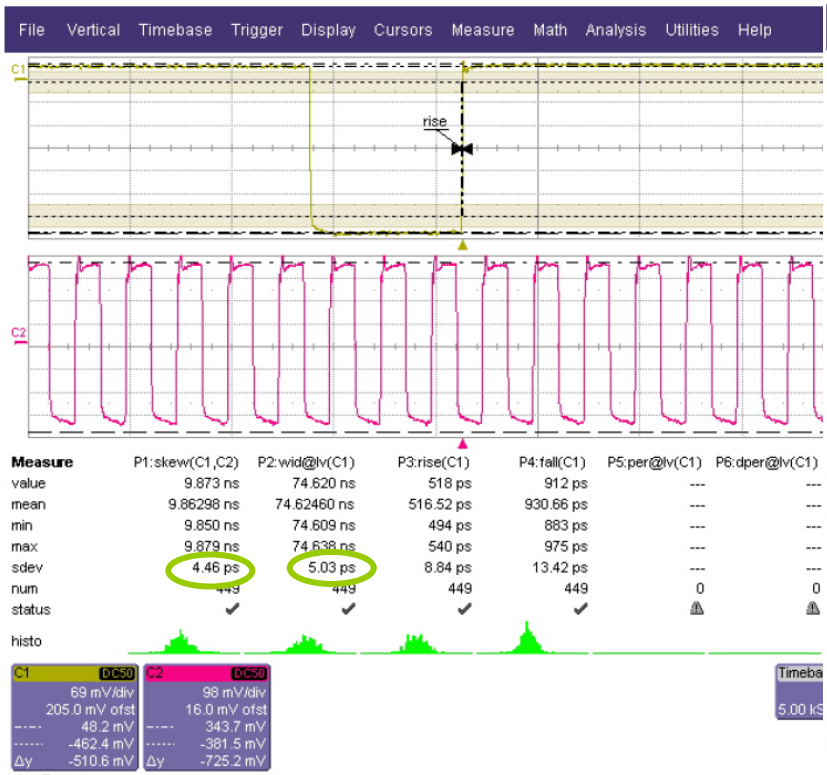
File Vertical Timebase Trigger Display Cursors Measure Math Analysis Utilities Help
rise
C1
C2
Measure P1:skew(C1,C2) P2:width(C1) P3:rise(C1) P4:fall(C1) P5:per@lv(C1) P6:dper@
value 10.024 ns 75.297 ns 455 ps 568 ps ---
mean 10.03265 ns 75.30241 ns 454.50 ps 564.81 ps ---
min 10.022 ns 75.288 ns 436 ps 524 ps ---
max 10.065 ns 75.318 ns 473 ps 642 ps ---
sdev 4.74 ps 5.52 ps 7.97 ps 20.27 ps ---
num 162 162 162 162 0
status ✔ ✔ ✔ ✔ ⚠
histo
C1 DC50 120 mV/div -380.0 mV 819 mV -75 mV Δy -894 mV
C2 DC50 98 mV/div 16.0 mV ofst 342.7 mV -387.4 mV Δy -730.1 mV

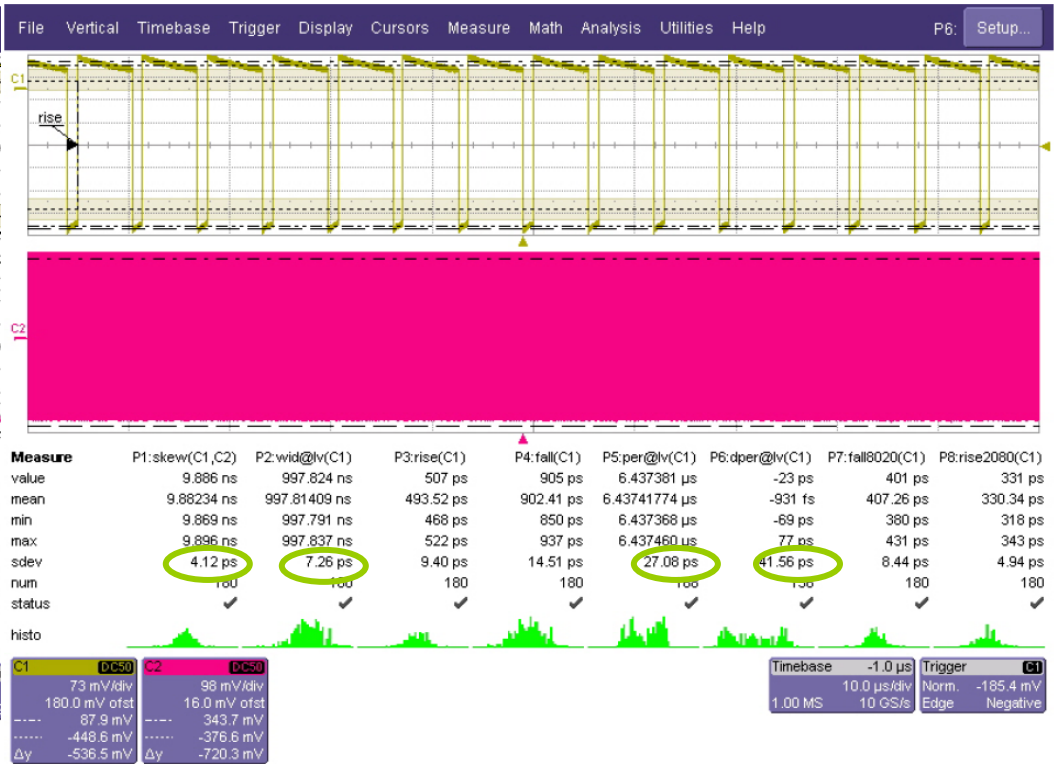

File Vertical Timebase Trigger Display Cursors Measure Math Analysis Utilities Help P6: Setup...
rise
C1
C2
Measure P1:skew(C1,C2) P2:wid@lv(C1) P3:rise(C1) P4:fall(C1) P5:per@lv(C1) P6:dper@lv(C1) P7:fall8020(C1) P8:rise2080(C1)
value 10.064 ns 998.528 ns 471 ps 642 ps 6.437387 µs -19 ps 362 ps 317 ps
mean 10.06100 ns 998.52637 ns 475.91 ps 624.27 ps 6.43741858 µs 1.19 ps 369.58 ps 313.39 ps
min 10.050 ns 998.512 ns 454 ps 575 ps 6.437373 µs -71 ps 348 ps 301 ps
max 10.074 ns 998.546 ns 505 ps 709 ps 6.437461 µs 54 ps 390 ps 326 ps
sdev 5.19 ps 7.86 ps 11.13 ps 24.85 ps 25.65 ps 39.40 ps 7.65 ps 5.06 ps
num 63 63 63 63 54 45 63 63
status ✔ ✔ ✔ ✔ ✔ ✔ ✔ ✔
histo
C1 DC50 108 mV/div -280.0 mV 676 mV -117 mV Δy -794 mV
C2 DC50 98 mV/div 16.0 mV ofst 343.7 mV -376.6 mV Δy -720.3 mV
Timebase 500 ns 5.00 µs/div 500 kS 10 GS/s
Trigger C1 Normal 116 mV Edge Negative

RF2TTC [Orbits]

- Internal orbit
  - Negative pulse
  - 3BC and 40BC wide pulse

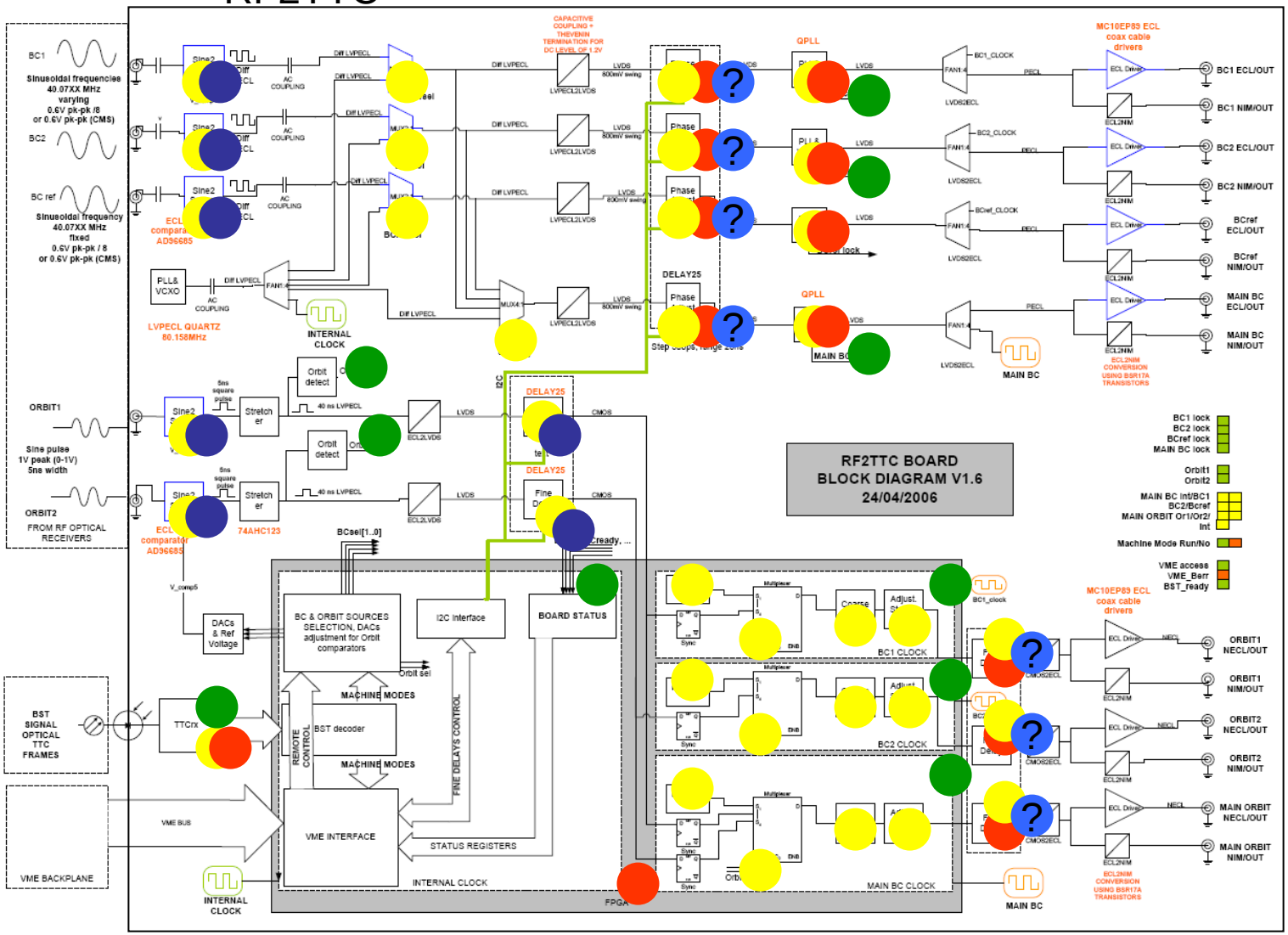



File Vertical Timebase Trigger Display Cursors Measure Math Analysis Utilities Help
C1
rise
C2
Measure P1:skew(C1,C2) P2:wid@lv(C1) P3:rise(C1) P4:fall(C1) P5:per@lv(C1) P6:dper@lv(C1)
value 9.873 ns 74.620 ns 518 ps 912 ps --- ---
mean 9.86298 ns 74.62460 ns 516.52 ps 930.66 ps --- ---
min 9.850 ns 74.609 ns 494 ps 883 ps --- ---
max 9.879 ns 74.638 ns 540 ps 975 ps --- ---
sdev 4.46 ps 5.03 ps 8.84 ps 13.42 ps --- ---
num 449 449 449 449 0 0
status
histo
C1 DC50 69 mV/div 205.0 mV ofst 48.2 mV -462.4 mV Δy -510.6 mV
C2 DC50 98 mV/div 16.0 mV ofst 343.7 mV -381.5 mV Δy -725.2 mV
Timeba
5.00 kS

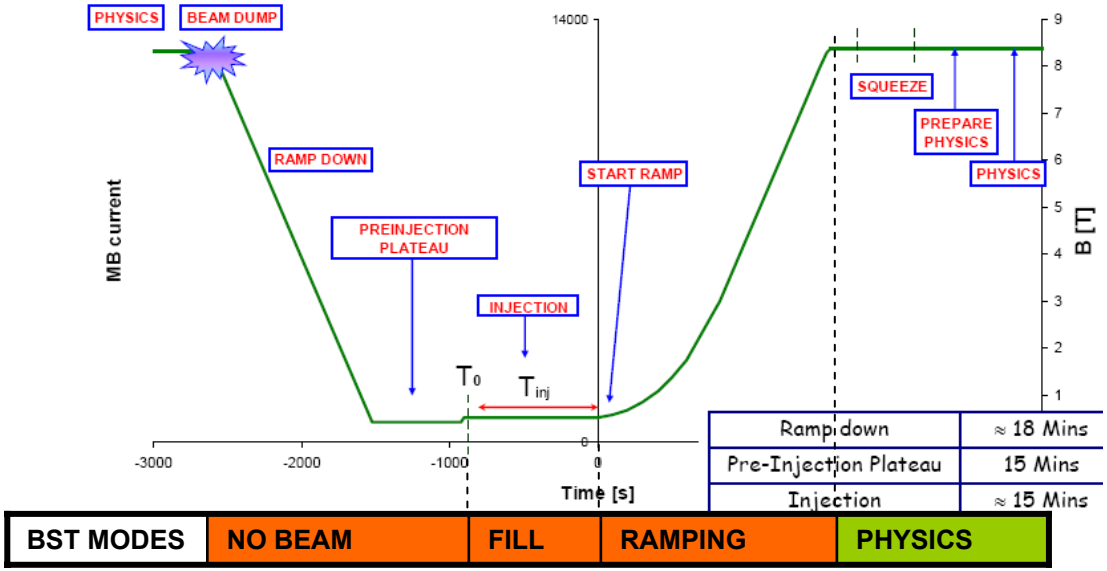

File Vertical Timebase Trigger Display Cursors Measure Math Analysis Utilities Help P6: Setup...
C1
rise
C2
Measure P1:skew(C1,C2) P2:wid@lv(C1) P3:rise(C1) P4:fall(C1) P5:per@lv(C1) P6:dper@lv(C1) P7:fall8020(C1) P8:rise2080(C1)
value 9.886 ns 997.824 ns 507 ps 905 ps 6.437381 µs -23 ps 401 ps 331 ps
mean 9.88234 ns 997.81409 ns 493.52 ps 902.41 ps 6.43741774 µs -931 fs 407.26 ps 330.34 ps
min 9.869 ns 997.791 ns 468 ps 850 ps 6.437368 µs -69 ps 380 ps 318 ps
max 9.896 ns 997.837 ns 522 ps 937 ps 6.437460 µs 77 ps 431 ps 343 ps
sdev 4.12 ps 7.26 ps 9.40 ps 14.51 ps 27.08 ps 41.56 ps 8.44 ps 4.94 ps
num 180 180 180 180 180 180 180 180
status
histo
C1 DC50 73 mV/div 180.0 mV ofst 87.9 mV -448.6 mV Δy -536.5 mV
C2 DC50 98 mV/div 16.0 mV ofst 343.7 mV -376.6 mV Δy -720.3 mV
Timebase -1.0 µs 10.0 µs/div 1.00 MS 10 GS/s
Trigger C1 Norm. -185.4 mV Edge Negative

RF2TTC [VME control & monitoring]

RF2TTC



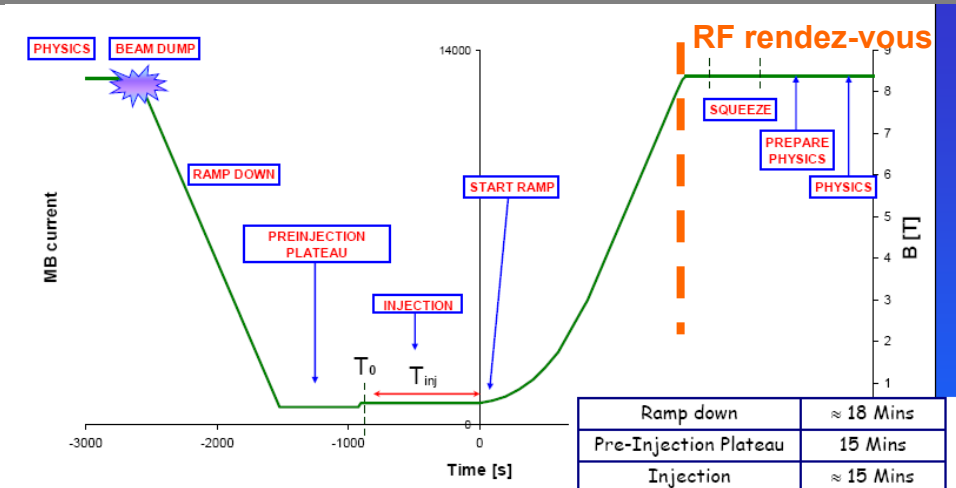
RF2TTC [working modes]



- The machine states are received through the BST signal
  - They are stored in a readable register
- The selection of each signal can be
  - Manual: independently from the machine states
  - Automatic: linked to the machine states (BST modes), following a configurable look-up table

RF2TTC [orbits synchronisation]

- Orb1in is synchronised to BC1in
- Orb2in is synchronised to BC2in
- Synchronisation in the RF2TTC:
  - Orb1out re-synchronised to BC1out
  - Orb2out re-synchronised to BC2out
  - OrbMainOut is Orb1 or Orb2 synchronised to BCmainOut
    - BCmain out = BC1, BC2, BCref or BCint
  - Ramping:
    - If BCref is used as a BCmain, the period of OrbMainOut will vary during the ramping, until the RF “rendez-vous”
    - Second option, use the internal orbit until the end of the ramping mode.



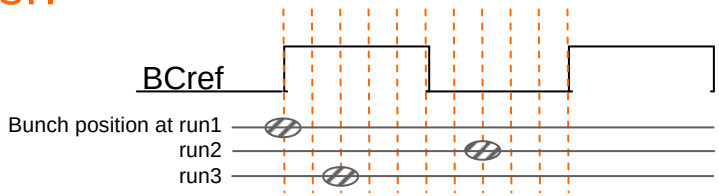
LHCOP: http://www.cern.ch/lhc-commissioning

Ramp down	≈ 18 Mins
Pre-Injection Plateau	15 Mins
Injection	≈ 15 Mins
Ramp	≈ 28 Mins
Squeeze	< 5 Mins
Prepare Physics	≈ 10 Mins
Physics	10 - 20 Hrs

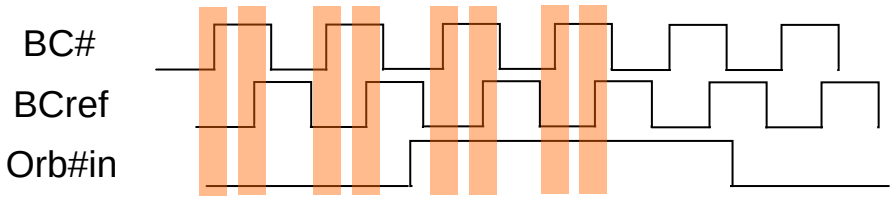
PROTONS - RAMPING = 28 minutes				
		Injection	**Physics**	**Δ**
BC	**Freq**	40.0788790 MHz	40.0789658 MHz	87 Hz
	Per	24.950798ns	24.950743ns	0.054 ps
Orbit	**Freq**	11.245477kHz	11.245501kHz	
	Per	88.924643us	88.924450us	193ps
IONS - RAMPING = 28 minutes				
		Injection	**Physics**	**Δ**
BC	**Freq**	40.0784139 MHz	40.0789639 MHz	550 Hz
	Per	24.951087ns	24.950745 ns	342 ps
Orbit	**Freq**	11.245346kHz	11.245501kHz	
	Per	88.925676us	88.924451us	1.225ns

RF2TTC [orbits phase relative to BC]

- During ramping the phase between orbit and BCref will vary (193ps for protons, 1.2ns for ions)
- After the RF “rendez-vous” (BC1 and BC2 synchronised to BCref), the phase between the bunch and the BC rising edge is normally different from one run to another:



  - It will be smoothly shifted after the rendez-vous to be situated always at the same position
  - The electronics to do that is under development, but may not be ready for the pilot run
  - Until this is ready, the orbit delay can be recalibrated at the beginning of each run using the orbit synchronisation in the RF2TTC
- If BCref is used as the BCmain during physics, the delay adjustment of the incoming orbit# must take into account its relative phases to BC# and BCref after re-sync



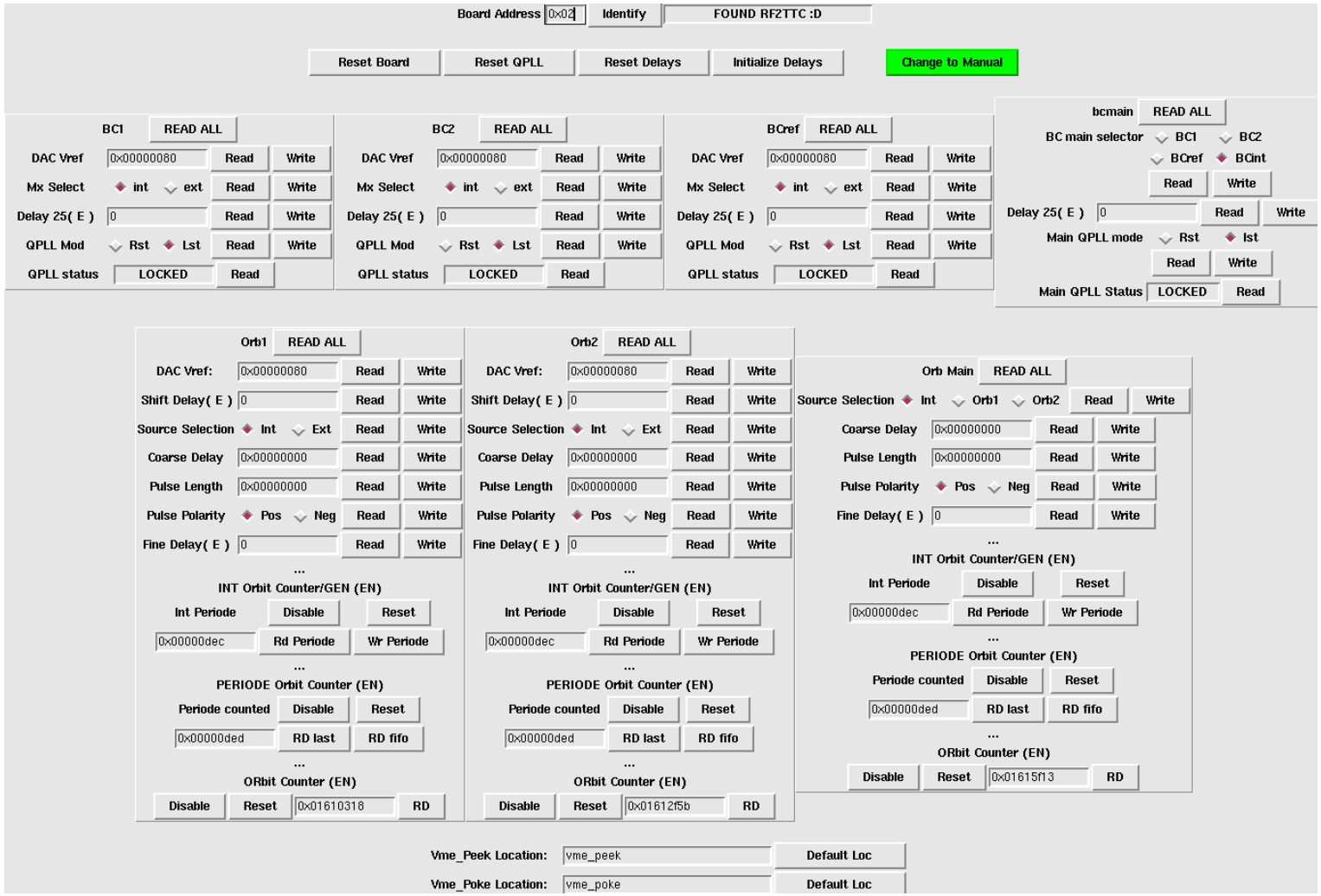
RF2TTC [software integration]

cctlinux01.cern.ch - PuTTY
Select an option:
1 Help
2 Raw register dump
3 Decode registers
4 Resets
5 Commands
6 Modify a register
7 Read CR/CSR registers
8 Write CSR registers
9 Dump the CR registers
10 Dump the CSR registers
11 VME peek
12 VME poke
13 Check structure
14 Set debugging parameters
0 Quit
Your choice: [2] :3
Decoding BC1 registers
BC source in manual mode: LHC BC
BC source in beam mode: LHC BC
BC source in no beam mode: LHC BC
QPLL locking mode: relock if lock is lost
Input comparator threshold: 0.000000 V
QPLL status: locked
Decoding BC2 registers
BC source in manual mode: LHC BC
BC source in beam mode: LHC BC
BC source in no beam mode: LHC BC
QPLL locking mode: relock if lock is lost
Input comparator threshold: 0.000000 V
QPLL status: locked
Decoding BCref registers
BC source in manual mode: LHC BC
BC source in beam mode: LHC BC
BC source in no beam mode: LHC BC
QPLL locking mode: relock if lock is lost
Input comparator threshold: 0.000000 V
QPLL status: locked

- Software API developed by M. Joos, in contact with:
  - ALICE: A. Justko
  - ATLAS: T. Pauly and C. Ohm
  - CMS: A. G. Holzner, J. Troska
  - LHCb: R. Jacobsson
- Simple functions
- Calibration routines
  - Orbit phase adjustment
  - Orbit threshold voltage
- Software ‘rf2ttcscope’ developed for
  - CCT VP110/317
  - CAEN PCI-controller card A2818
  - CAEN V1718 VME-USB bridge
- Last version updated on CVS repository

RF2TTC [test panel]

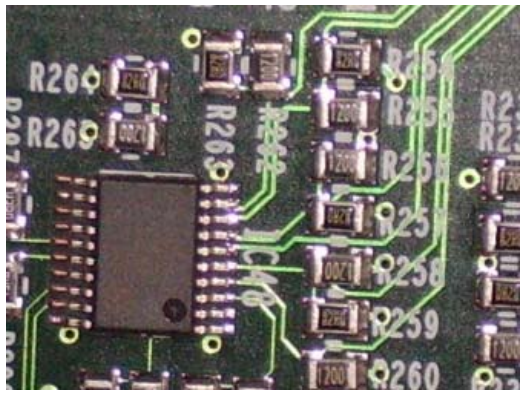
- Developed for CCT crate controllers

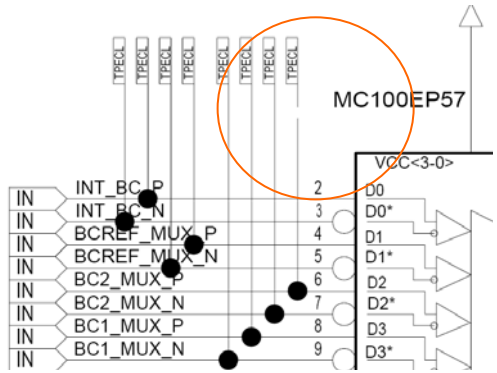

Board Address 0x02
Identify
FOUND RF2TTC :D
Reset Board
Reset QPLL
Reset Delays
Initialize Delays
Change to Manual
BC1
READ ALL
DAC Vref 0x00000080 Read Write
Mx Select int ext Read Write
Delay 25(E) 0 Read Write
QPLL Mod Rst Lst Read Write
QPLL status LOCKED Read
BC2
READ ALL
DAC Vref 0x00000080 Read Write
Mx Select int ext Read Write
Delay 25(E) 0 Read Write
QPLL Mod Rst Lst Read Write
QPLL status LOCKED Read
BCref
READ ALL
DAC Vref 0x00000080 Read Write
Mx Select int ext Read Write
Delay 25(E) 0 Read Write
QPLL Mod Rst Lst Read Write
QPLL status LOCKED Read
bcmain
READ ALL
BC main selector BC1 BC2 BCref BCint
Read Write
Delay 25(E) 0 Read Write
Main QPLL mode Rst Ist
Read Write
Main QPLL Status LOCKED Read
Orb1
READ ALL
DAC Vref: 0x00000080 Read Write
Shift Delay(E) 0 Read Write
Source Selection Int Ext Read Write
Coarse Delay 0x00000000 Read Write
Pulse Length 0x00000000 Read Write
Pulse Polarity Pos Neg Read Write
Fine Delay(E) 0 Read Write
INT Orbit Counter/GEN (EN)
Int Periode Disable Reset
0x00000dec Rd Periode Wr Periode
PERIODE Orbit Counter (EN)
Periode counted Disable Reset
0x00000ded RD last RD fifo
ORbit Counter (EN)
Disable Reset 0x01610318 RD
Orb2
READ ALL
DAC Vref: 0x00000080 Read Write
Shift Delay(E) 0 Read Write
Source Selection Int Ext Read Write
Coarse Delay 0x00000000 Read Write
Pulse Length 0x00000000 Read Write
Pulse Polarity Pos Neg Read Write
Fine Delay(E) 0 Read Write
INT Orbit Counter/GEN (EN)
Int Periode Disable Reset
0x00000dec Rd Periode Wr Periode
PERIODE Orbit Counter (EN)
Periode counted Disable Reset
0x00000ded RD last RD fifo
ORbit Counter (EN)
Disable Reset 0x01612f5b RD
Orb Main
READ ALL
Source Selection Int Orb1 Orb2 Read Write
Coarse Delay 0x00000000 Read Write
Pulse Length 0x00000000 Read Write
Pulse Polarity Pos Neg Read Write
Fine Delay(E) 0 Read Write
INT Orbit Counter/GEN (EN)
Int Periode Disable Reset
0x00000dec Rd Periode Wr Periode
PERIODE Orbit Counter (EN)
Periode counted Disable Reset
0x00000ded RD last RD fifo
ORbit Counter (EN)
Disable Reset 0x01615f13 RD
Vme_Peek Location: vme_peek Default Loc
Vme_Poke Location: vme_poke Default Loc

RF2TTC [work with the users]

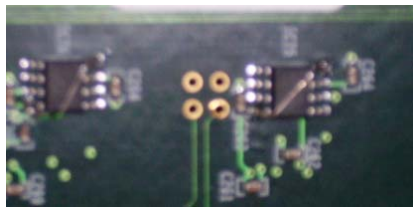
- ATLAS (T. Pauly and C. Ohm) used the board during 15 days
  - Noticed a few bugs that have been solved
  - So far, no extra functionality has been required
- CMS to take over this week
- LHCb during the 2 last weeks of February

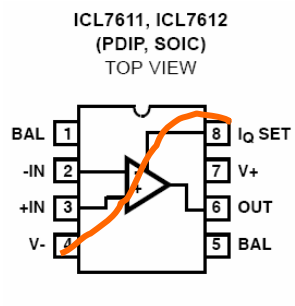
- A few bugs to solve
  - Missing termination on one line

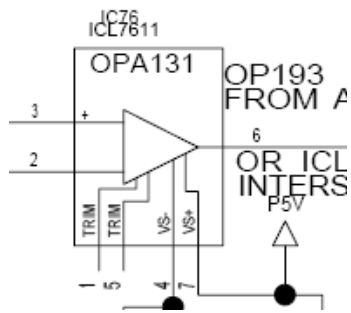




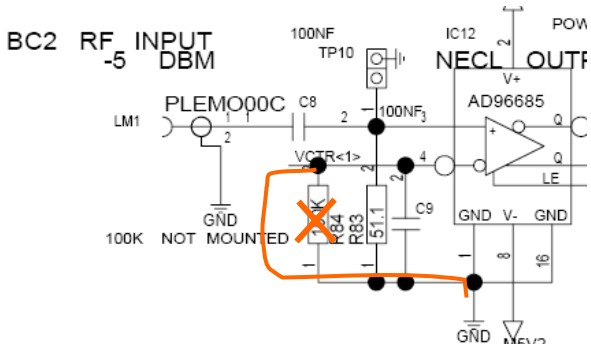
  - Missing wire on orbit DAC reference level







  - Remove the adjustment for clock threshold



RF2TTC [from V2 to V3]

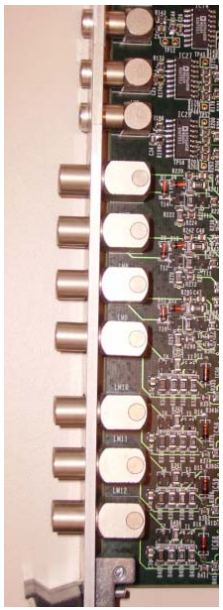
BC2
BCref
BC1

Orb2
Orb1

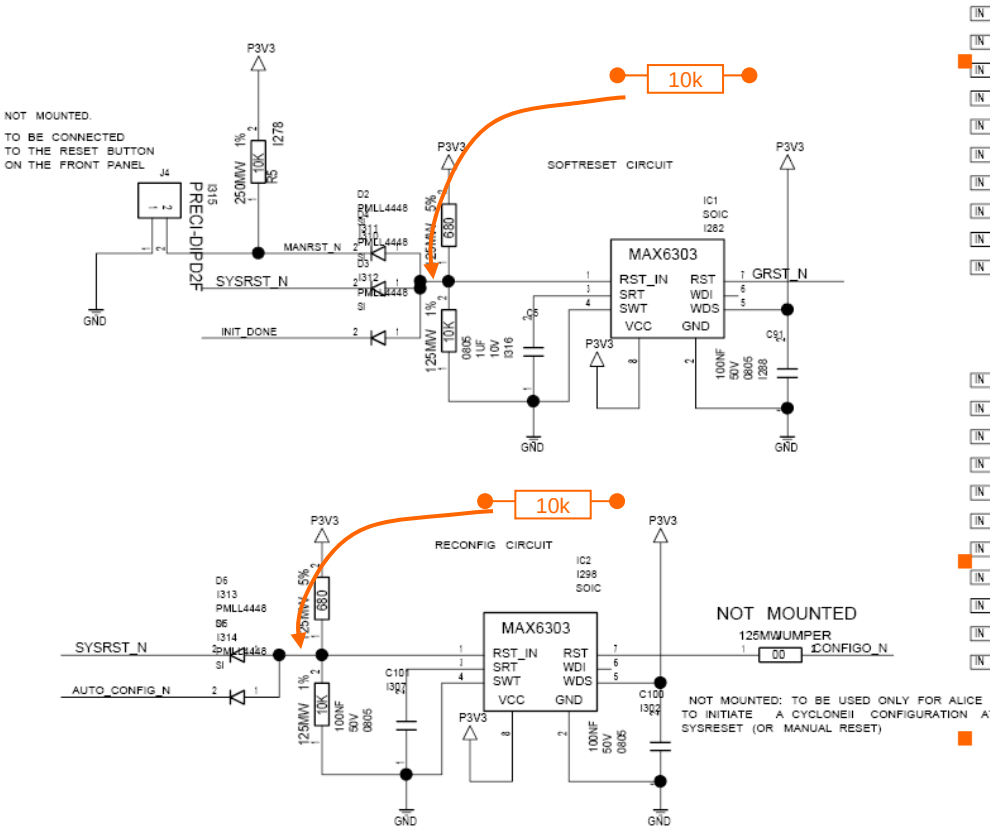
OrbMain
Orb2
Orb1
BCMain

BCref
BC2
BC1

- Improve the front panel
  - Fancy inputs and outputs positionning
  - Align inputs and output lemo connectors if possible



RF2TTC [from V2 to V3]



Reset

- Activated via
  - Sysrst_n
  - Manual reset? (no place for a reset button on the patch panel)
  - During FPGA configuration
  - Via VME access
    - Global reset
    - Partial resets
- Add a resistor for current control

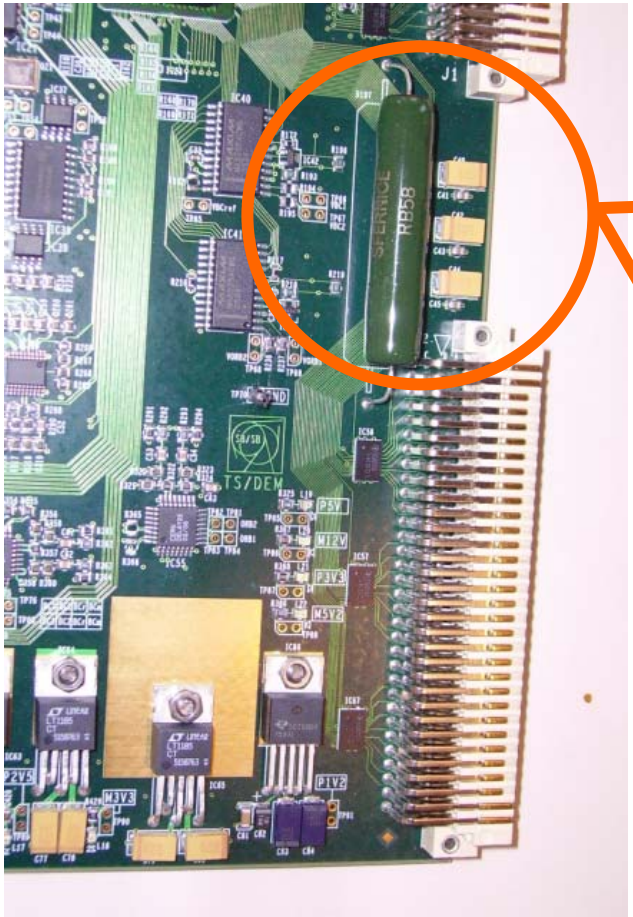
FPGA reconfiguration

- After a sysreset? ☹
- Write access to a special register?

Automatic chips initialisation after power-up

- CMS request
- Once the FPGA configuration is done (using the active level of the init_done signal)
- Requires assigning a new pin to the fpga

RF2TTC [from V2 to V3]



- -12V to -5V conversion
  - Try to optimise the regulator heat and the voltage drop
  - Ugly and HOT (120 deg) !

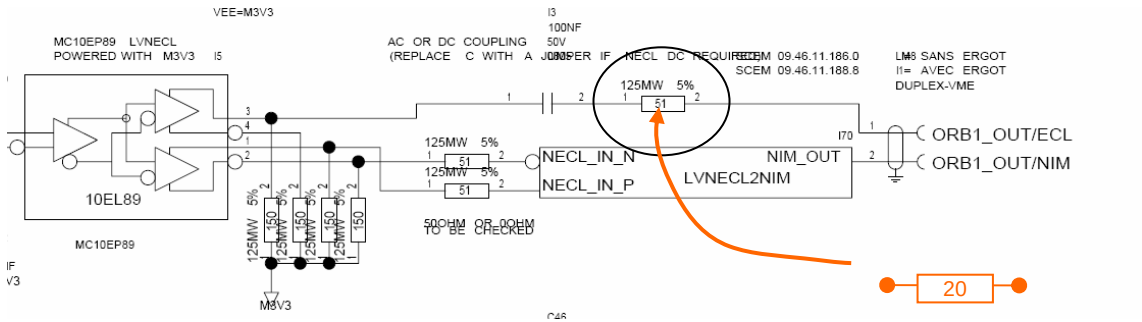
Connaissez-vous les 3 gestes d'urgence ?

1 » **Si la brûlure n'est pas trop étendue, rincez immédiatement et abondamment avec de l'eau froide** pendant au moins 5 minutes et à 15 cm du robinet. Pourquoi de l'eau froide ? Parce qu'elle refroidit la zone brûlée, elle limite la douleur et elle protège la brûlure en évitant de percer la cloque. De plus, dans le cas d'une brûlure par produit chimique, l'eau froide permet de limiter l'extension en taille et en profondeur de la plaie.

2 » **Enveloppez la brûlure dans un linge humide et propre**. Surtout, n'appliquez jamais de pommade, de corps gras ou même des glaçons.

3 » **Surveillez la brûlure**. Si elle devient à nouveau chaude, qu'elle gonfle, qu'elle est encore douloureuse dans les 24 heures, bref, au moindre doute, consultez un médecin.

RF2TTC [from V2 to V3]



- Output signal level – MC10EP89 – ECL coax driver
  - Adjust the serial resistor to adjust the ECL level at the receiver
    - With 50 Ohm:
      - BC out = 650mV
      - Pos Orb out = 750 mV
      - Neg Orb out = 480 mV
    - With 0 Ohm:
      - BCout = 1.1V
      - Pos Orb out = 1.4V
      - Neg Orb out = 600 mV

    ⇒ 20 Ohm probably is the best compromise

    ⇒ Replace 125mW 150Ohm resistors with 250mW

    ⇒ Not the same problem with the fanout, which has his drivers powered with VCC= 5V. Their output swing is higher (Pos Orb= 900mV, Neg Orb = 830mV).

RF2TTC [from V2 to V3]

- Missing firmware
  - Init after reconfiguration
    - Which default values?
      - Internal or external signals?
      - Delays adjustment necessarily not adjusted
  - FPGA reconfiguration by accessing a VME register
  - Eprom reprogramming via VME and .jam files
- General questions
  - Minimum orbit out length = 3bc. Is it ok?

RF2TTC [quantities & price estimation]

- 3 RF2TTC modules per experiment
  - 1 in use
  - 1 hot spare
  - 1 cold spare*
- 3 for the TTC support*
- PCB and components for 10 more spares*

- Quantities & price per experiment (to be discussed)

Quantities per exp	Used	Hot Spares	Cold Spares	Unassembled spares	Unit price	Total quantities	Total Price kCHF
RF2TTC	1	1	1*	2*	2.5	3	7.5 kCHF

* Managed by TTC support

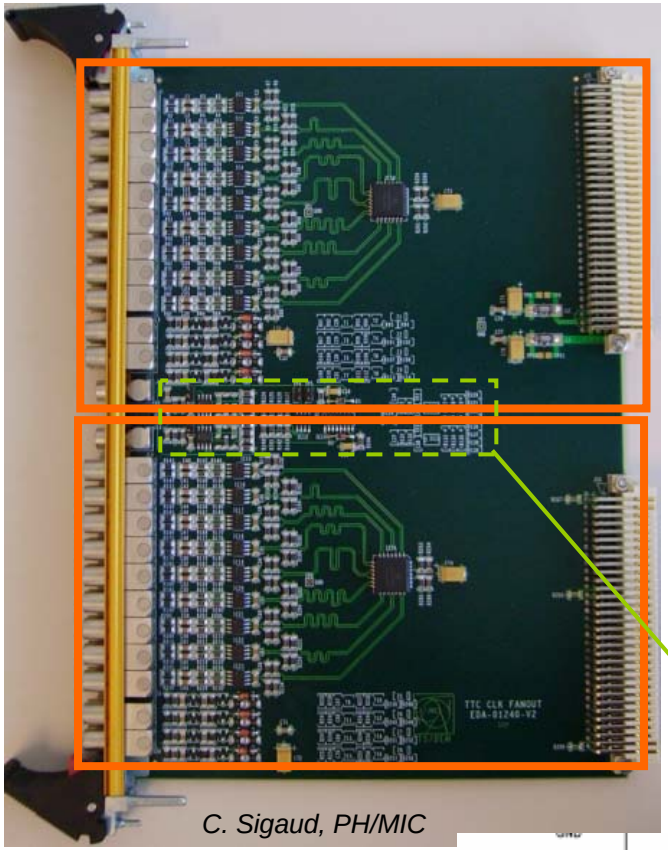
RF2TTC [schedules]

	FEBRUARY			MARCH				APRIL				MAY			
Version2 User tests															
Schematics															
Layout															
Pre-production															
Pre-prod tests															
Production															
Production tests												*			
Module distribution															

*** Including ageing using the climatic chamber**

- System overview
- Optical Tx and Rx modules
- RF2TTC module
- Fanout
  - Overview
  - Performances
- TTC Crate
- Full system
- Documentation
- AOB

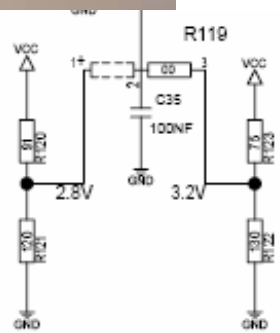
FANOUT [overview]

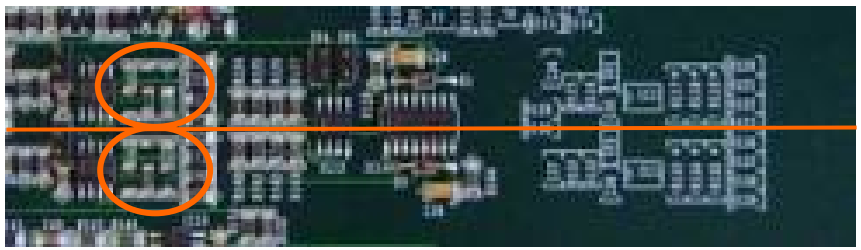


EDA-01240

- 2 identical parts of
  - 1:18 ECL fanout
  - 4 NIM copies
  - Identical delay for all the output
- Can be daisy-chained to be a
  - 1:35 ECL fanout
  - 8 NIM copies
- Deals with:
  - Clocks
  - Positive ECL orbit
  - Negative ECL orbit

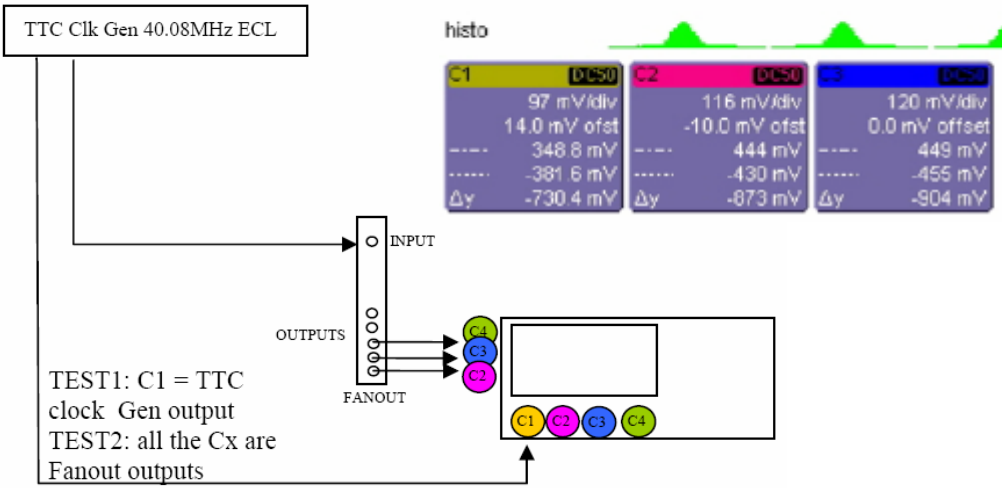
  … by changing one resistor
- Possibility to invert the signal (changing 2 SMD resistors)





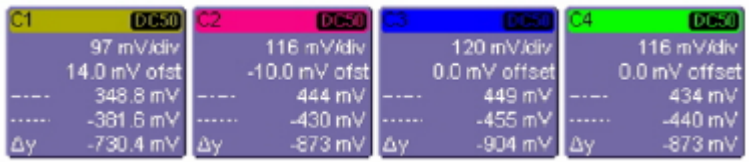
FANOUT [40MHz]

Measure	P1:skew(C1,C2)	P2:skew(C1,C3)	P3:dper@lv(C1)	P4:dper@lv(C2)	P5:dper@lv(C3)	P6:per@lv(C1)	P7:per@lv(C2)	P8:per@lv(C3)
value	6.276 ns	6.206 ns	-32 ps	3 ps	-6 ps	24.931 ns	24.953 ns	24.948 ns
mean	6.26450 ns	6.20140 ns	-1 fs	0 fs	0 fs	24.95112 ns	24.95112 ns	24.95112 ns
min	6.234 ns	6.173 ns	-64 ps	-28 ps	-32 ps	24.918 ns	24.934 ns	24.933 ns
max	6.297 ns	6.235 ns	61 ps	29 ps	30 ps	24.985 ns	24.970 ns	24.969 ns
sdev	7.42 ps	7.39 ps	15.39 ps	7.19 ps	7.61 ps	9.03 ps	4.30 ps	4.48 ps
num	36.063e+3	36.063e+3	36.045e+3	36.054e+3	36.054e+3	36.054e+3	36.063e+3	36.063e+3
status	✔	✔	✔	✔	✔	✔	✔	✔
histo								



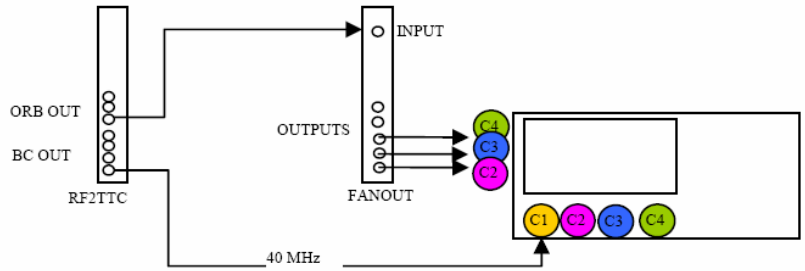
C1= TTC Clock Gen reference
C2, C3, C4 = Fanout outputs

Measure	P1:skew(C1,C2)	P2:skew(C2,C3)	P3:skew(C1,C3)	P4:skew(C1,C4)	P5:skew(C3,C4)	P6:skew(C2,C4)	P7:per@lv(C2)	P8:per@lv(C3)
value	45 ps	-40 ps	1 ps	50 ps	50 ps	9 ps		
mean	44.20 ps	-41.99 ps	3.38 ps	52.03 ps	48.34 ps	11.04 ps		
min	30 ps	-60 ps	-12 ps	37 ps	31 ps	-7 ps		
max	59 ps	-26 ps	18 ps	67 ps	65 ps	29 ps		
sdev	3.50 ps	4.06 ps	3.60 ps	3.67 ps	4.16 ps	4.12 ps		
num	56.084e+3	56.084e+3	56.084e+3	56.084e+3	56.084e+3	56.084e+3		
status	✔	✔	✔	✔	✔	✔		
histo								



C1, C2, C3, C4 = Fanout outputs

FANOUT [orbit]

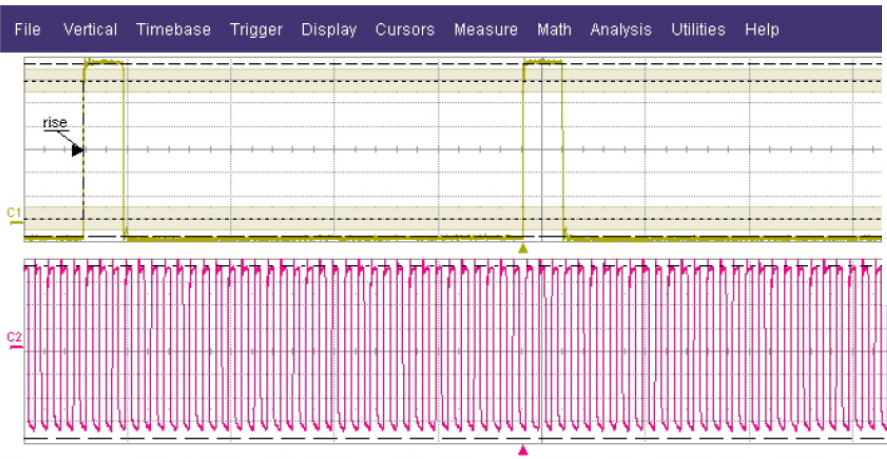


Measure	P1:skew(C1,C2)	P2:wid@lv(C1)	P3:rise(C1)	P4:fall(C1)	P5:per@lv(C1)	P6:dper@lv(C1)	P7:fall8020(C1)	P8:rise2080(C1)
value	4.997 ns	998.843 ns	777 ps	568 ps	6.437431 µs	-15 ps	372 ps	415 ps
mean	5.00462 ns	998.85457 ns	796.89 ps	575.42 ps	6.43741661 µs	154 fs	376.03 ps	417.71 ps
min	4.994 ns	998.832 ns	684 ps	541 ps	6.437371 µs	-74 ps	359 ps	396 ps
max	5.019 ns	998.874 ns	907 ps	611 ps	6.437465 µs	69 ps	392 ps	443 ps
sdev	5.64 ps	9.22 ps	50.56 ps	11.88 ps	26.89 ps	40.66 ps	6.86 ps	9.23 ps
num	91	91	91	91	78	65	91	91
status	✔	✔	✔	✔	✔	✔	✔	✔
histo								

C1 DC50	C2 DC50
128 mV/div	98 mV/div
-320.0 mV	16.0 mV ofst
790 mV	343.7 mV
-151 mV	-376.6 mV
Δy -941 mV	Δy -720.3 mV

Timebase	500 ns
	5.00 µs/div
500 kS	10 GS/s

Trigger	C1
Normal	127 mV
Edge	Negative



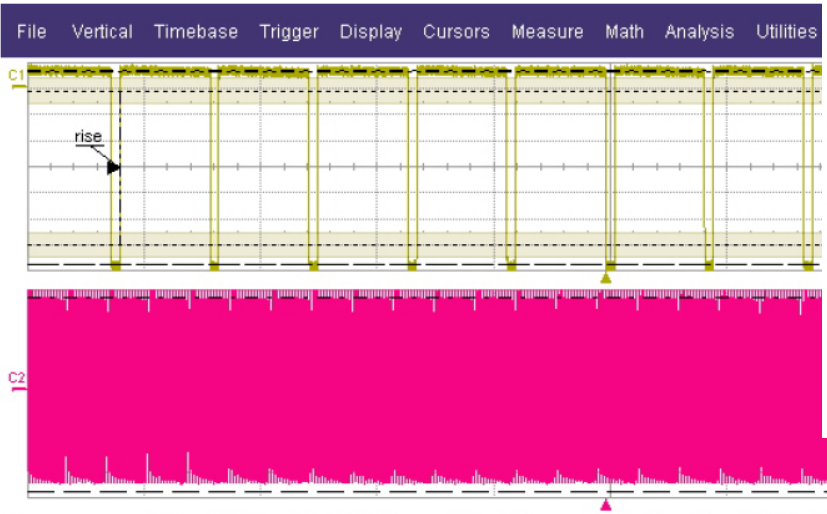
Measure	P1:skew(C1,C2)	P2:width(C1)	P3:rise(C1)	P4:fall(C1)	P5:per@lv(C1)	P6:dper@lv(C1)	P7:per@lv(C2)	P8:per@lv(C3)
value	4.995 ns	75.926 ns	516 ps	512 ps	848.343 ns	10 ps		
mean	4.99915 ns	75.92334 ns	515.42 ps	496.41 ps	848.34236 ns	1.42 ps		
min	4.986 ns	75.911 ns	491 ps	474 ps	848.322 ns	-20 ps		
max	5.012 ns	75.937 ns	540 ps	520 ps	848.363 ns	20 ps		
sdev	5.08 ps	6.07 ps	9.61 ps	9.33 ps	7.16 ps	9.19 ps		
num	159	159	159	159	106	53		
status	✔	✔	✔	✔	✔	✔		
histo								

C1 DC50	C2 DC50
120 mV/div	98 mV/div
-380.0 mV	16.0 mV ofst
820 mV	343.7 mV
-68 mV	-381.5 mV
Δy -888 mV	Δy -725.2 mV

Timebase	-36 ns
	200 ns/div
20.0 kS	10 GS/s

Trigger	C1
Normal	-1 mV
Edge	Positive

FANOUT [orbit]



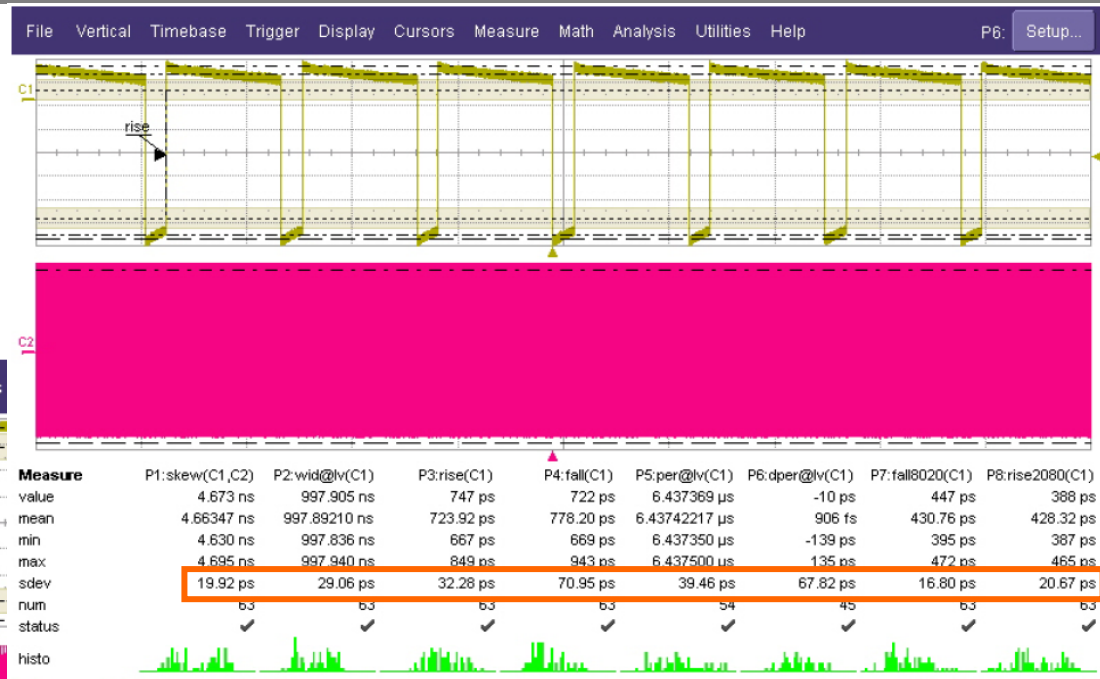
Measure	P1:skew(C1,C2)	P2:wid@lv(C1)	P3:rise(C1)	P4:fall(C1)	P5:per@lv(C1)	P6:dper@lv(C1)	P7:fall8020(C1)	P8:rise2080(C1)
value	4.549 ns	74.819 ns	807 ps	873 ps	848.304 ns	-72 ps	455 ps	417 ps
mean	4.55544 ns	74.78567 ns	776.02 ps	895.31 ps	848.34234 ns	28 fs	438.58 ps	440.23 ps
min	4.504 ns	74.723 ns	700 ps	721 ps	848.283 ns	-103 ps	396 ps	387 ps
max	4.597 ns	74.847 ns	862 ps	1.094 ns	848.396 ns	111 ps	483 ps	506 ps
sdev	20.86 ps	31.89 ps	33.14 ps	74.22 ps	27.02 ps	51.76 ps	17.66 ps	20.31 ps
num	1.001e+3	1.001e+3	1.001e+3	1.001e+3	910	819	1.001e+3	1.001e+3
status	✔	✔	✔	✔	✔	✔	✔	✔
histo								

C1 DC50: 112 mV/div, 340.0 mV ofst, 71 mV, -758 mV, Δy -829 mV

C2 DC50: 98 mV/div, 16.0 mV ofst, 343.7 mV, -381.5 mV, Δy -725.2 mV

Timebase -40 ns, 1.00 µs/div, 100 kS, 10 GS/s

Trigger C1, Normal, Edge, -345 mV, Negative



Measure	P1:skew(C1,C2)	P2:wid@lv(C1)	P3:rise(C1)	P4:fall(C1)	P5:per@lv(C1)	P6:dper@lv(C1)	P7:fall8020(C1)	P8:rise2080(C1)
value	4.673 ns	997.905 ns	747 ps	722 ps	6.437369 µs	-10 ps	447 ps	388 ps
mean	4.66347 ns	997.89210 ns	723.92 ps	778.20 ps	6.43742217 µs	906 fs	430.76 ps	428.32 ps
min	4.630 ns	997.836 ns	667 ps	669 ps	6.437350 µs	-139 ps	395 ps	387 ps
max	4.695 ns	997.940 ns	849 ps	943 ps	6.437500 µs	135 ps	472 ps	465 ps
sdev	19.92 ps	29.06 ps	32.28 ps	70.95 ps	39.46 ps	67.82 ps	16.80 ps	20.67 ps
num	63	63	63	63	54	45	63	63
status	✔	✔	✔	✔	✔	✔	✔	✔
histo								

C1 DC50: 124 mV/div, 280.0 mV ofst, 175 mV, -736 mV, Δy -911 mV

C2 DC50: 98 mV/div, 16.0 mV ofst, 343.7 mV, -376.6 mV, Δy -720.3 mV

Timebase -500 ns, 5.00 µs/div, 500 kS, 10 GS/s

Trigger C1, Normal, Edge, -304 mV, Negative

FANOUT [quantities & price estimation]

- Quantities:
  - ALICE:
  - ATLAS:
  - CMS:
  - LHCb:
  - TTC support: 2

- Price: 2.5 kCHF

- System overview
- Optical Tx and Rx modules
- RF2TTC module
- Fanout
- TTC Crate
- Full system
- Documentation
- AOB

TTC Crates [overview]

- Crates
  - Standard “LHC crates” (6U VME64x)
    - Already delivered to ATLAS, CMS, LHCb
  - Special water cooled crate for ALICE
    - Bin available, power supply delayed
- Crate Controllers
  - ALICE:
    - Standard VP315/317 from CCT
  - ATLAS:
    - Standard VP110 from CCT
    - Available
  - CMS:
    - CAEN PCI-controller card A2818 + V2718 VME-PCI optical bridge
    - Delivered
  - LHCb:
    - CAEN V1718 VME-USB bridge
    - Delivered

- System overview
- Optical Tx and Rx modules
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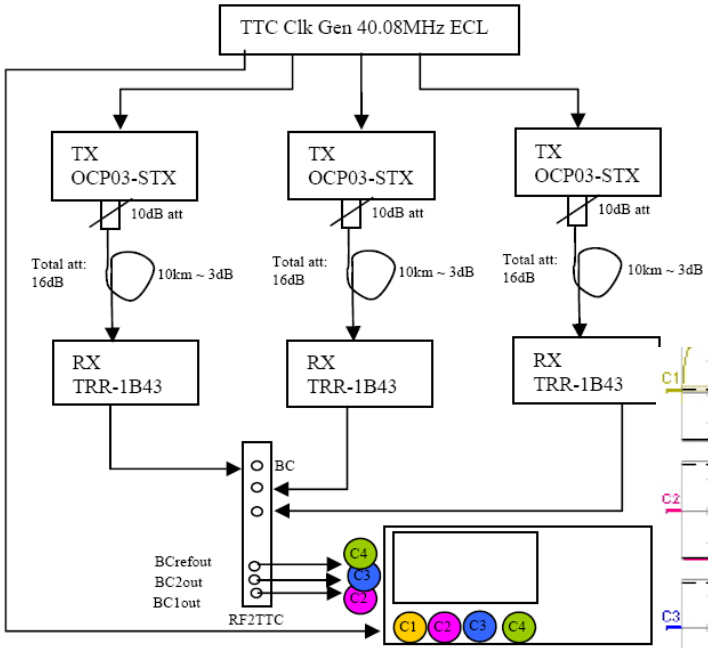
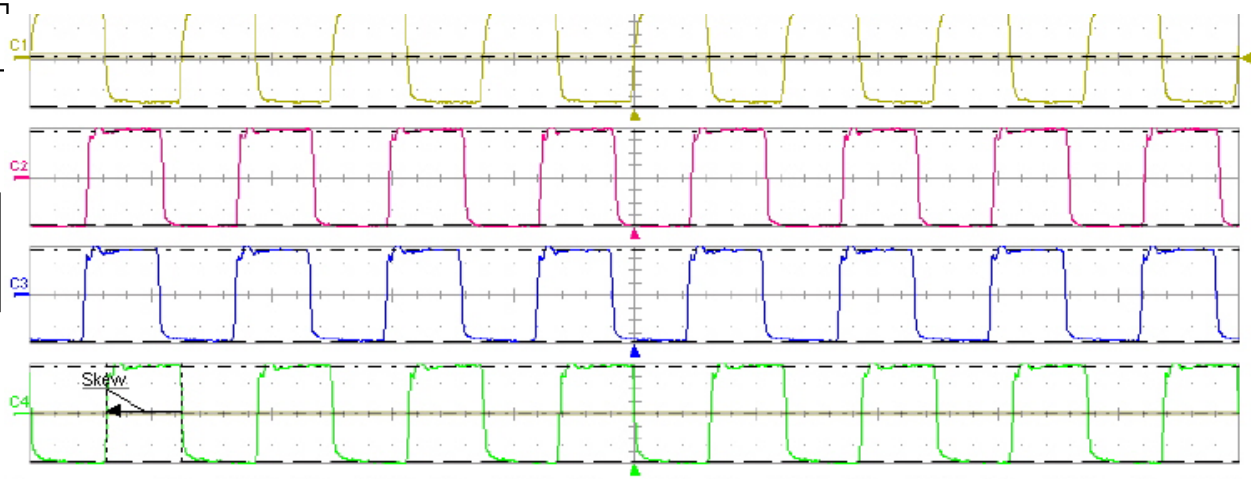
- TTC Crate
- Full system
  - Performances
  - Production quantities
  - Software
  - Price
  - Schedules
  - Maintenance & support
  - Summer plans
- Documentation
- AOB

FULL SYSTEM [concurrent 40MHz]

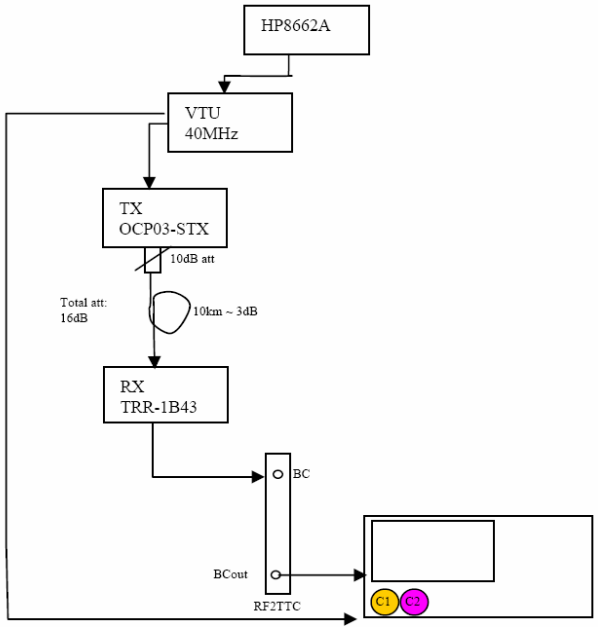




Measure	P1:skew(C1,C2)	P2:skew(C1,C3)	P3:skew(C1,C4)	P4:dper@lv(C1)	P5:dper@lv(C2)	P6:dper@lv(C3)	P7:dper@lv(C4)	P8:per@lv(C1)
value	9.447 ns	8.946 ns	-12.308 ns	-0 ps	-2 ps	3 ps	-1 ps	24.948 ns
mean	9.43745 ns	8.90919 ns	-12.32095 ns	146 fs	40 fs	7 fs	25 fs	24.95108 ns
min	9.362 ns	8.839 ns	-12.378 ns	-51 ps	-23 ps	-25 ps	-22 ps	24.921 ns
max	9.494 ns	8.965 ns	-12.256 ns	46 ps	26 ps	24 ps	22 ps	24.964 ns
sdev	15.14 ps	21.04 ps	17.46 ps	14.56 ps	6.60 ps	6.44 ps	6.13 ps	6.34 ps
num	7.210e+3	6.937e+3	6.643e+3	6.218e+3	5.416e+3	5.304e+3	5.178e+3	6.433e+3
status	✔	✔	✔	✔	✔	✔	✔	✔
histo								

C1 DC50 97 mV/div 14.0 mV ofst 348.8 mV -381.6 mV Δy -730.4 mV
C2 DC50 84 mV/div -9.0 mV offset 323.2 mV -309.4 mV Δy -632.5 mV
C3 DC50 90 mV/div 0.0 mV offset 336.6 mV -341.1 mV Δy -677.7 mV
C4 DC50 86 mV/div -1.0 mV offset 322.6 mV -324.9 mV Δy -647.6 mV
Timebase 0.0 ns 20.0 ns/div 2.00 kS 10 GS/s
Trigger C1 Normal -970 µV Edge Positive

FULL SYSTEM [individual 40MHz]



- BC1

	Skew versus ref	Cy2Cy	Frequency	Period	Duty Cycle
Ref Std Dev		11ps rms	10.27kHz rms	6.40ps rms	
Mean value			40.0799MHz	24.95ns	49.9%
Standard Dev	16.6ps rms	6.25ps rms	5.87kHz rms	3.65ps rms	0.014%
pkpk	110ps pkpk	42ps pkpk	50kHz pkpk	34ps pkpk	0.11% pkpk

- BC2

	Skew versus ref	Cy2Cy	Frequency	Period	Duty Cycle
Ref Std Dev		11ps rms	10.27kHz rms	6.40ps rms	
Mean value			40.0799MHz	24.95ns	49.8%
Standard Dev	21.7ps rms	6.07ps rms	5.65kHz rms	3.51ps rms	0.013%
pkpk	120ps pkpk	62ps pkpk	50kHz pkpk	32ps pkpk	0.11% pkpk

- BCref

	Skew versus ref	Cy2Cy	Frequency	Period	Duty Cycle
Ref Std Dev		11ps rms	10.27kHz rms	6.40ps rms	
Mean value			40.0799MHz	24.95ns	49.9%
Standard Dev	36ps rms	6.28ps rms	5.88kHz rms	3.66ps rms	0.012%
pkpk	154ps pkpk	57ps pkpk	50kHz pkpk	33ps pkpk	0.12% pkpk

High values for proto1 only
Proto2: BCref=19ps rms
BCmain on BCref = 21ps rms

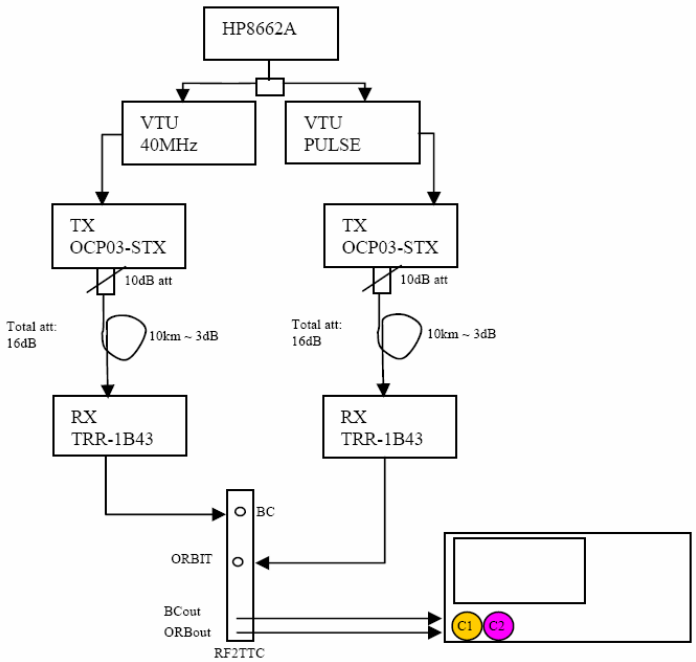
- BCmain on BC1

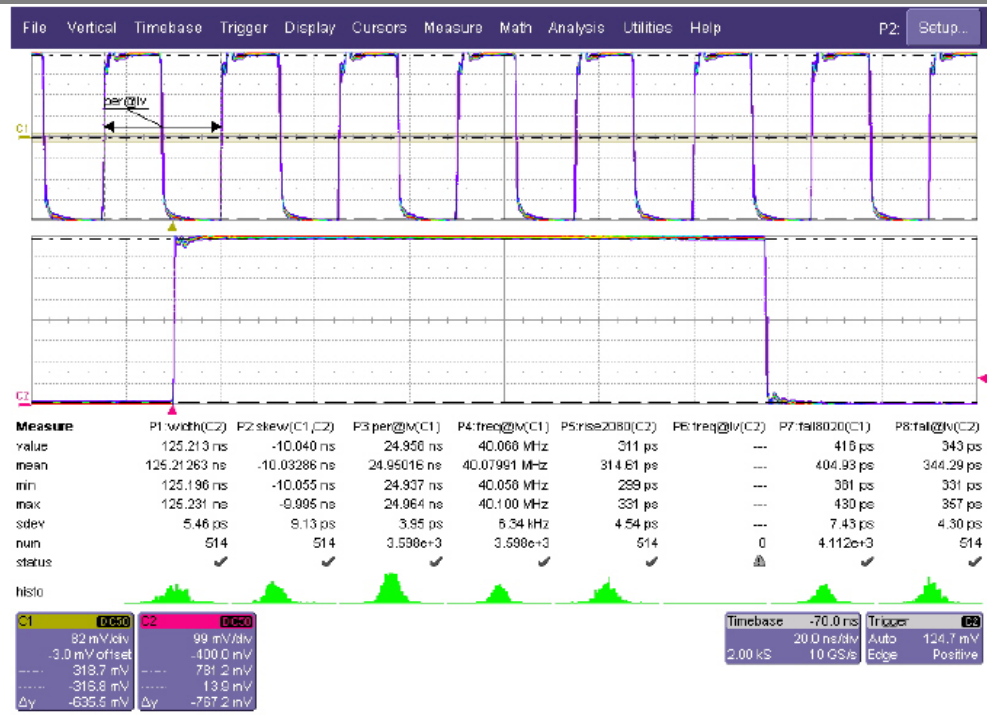
	Skew versus ref	Cy2Cy	Frequency	Period	Duty Cycle
Ref Std Dev		11ps rms	10.27kHz rms	6.40ps rms	
Mean value			40.0799MHz	24.95ns	49.8%
Standard Dev	17.9ps rms	5.99ps rms	5.61kHz rms	3.49ps rms	0.013%
pkpk	104ps pkpk	50ps pkpk	50kHz pkpk	32ps pkpk	0.11% pkpk

BCmain on BCref

	Skew versus ref	Cy2Cy	Frequency	Period	Duty Cycle
Ref Std Dev		11ps rms	10.27kHz rms	6.40ps rms	
Mean value			40.0799MHz	24.95ns	49.8%
Standard Dev	40.7ps rms	6.23ps rms	5.83kHz rms	3.63ps rms	0.012%
pkpk	198ps pkpk	50ps pkpk	49kHz pkpk	33ps pkpk	0.10% pkpk

FULL SYSTEM [40MHz & orbit]





	Output Pulse width	Skew of the Orbit_out versus BCout	Orbit rising edge	Orbit falling edge
Mean	125.2ns		312ps	405ps
Standard Deviation	5.43ps rms	9ps rms	4.73ps rms	7.45ps rms
Pkpk	30ps pkpk	60ps rms	50ps pkpk	42ps pkpk

FULL SYSTEM [performance conclusions]

Typical results of a full system

Bunch Clock			Orbit			
	Skew versus source	Cy2Cy	Output Pulse width	Skew of the Orbit_out versus BCout	Orbit rising edge	Orbit falling edge
Source Std Dev		11ps rms				
Std Dev	16.6ps rms	6.25ps rms	5.43ps rms	9ps rms	4.73ps rms	7.45ps rms
pkpk	110ps pkpk	42ps pkpk	30ps pkpk	60ps rms	50ps pkpk	42ps pkpk

- Still to be understood:
  - Why BCref skew jitter is ~40ps rms instead of 17ps rms on the RF2TTC proto1?
    - Only with the VTU generator
    - spectraQuest analysis didn't show anything
    - Jitter tracking on the board showed increased jitter only after the delay25
    - No problems seen on the second prototype

FULL SYSTEM [software]

- Complete API will provide
  - RF_Rx control and monitoring
  - RF2TTC control with calibration routines
  - Portability to CCT controllers and CAEN PCI/USB interfaces
- The frequency received by each Rx will be published on the DIP for the RF

FULL SYSTEM [quantities & price]

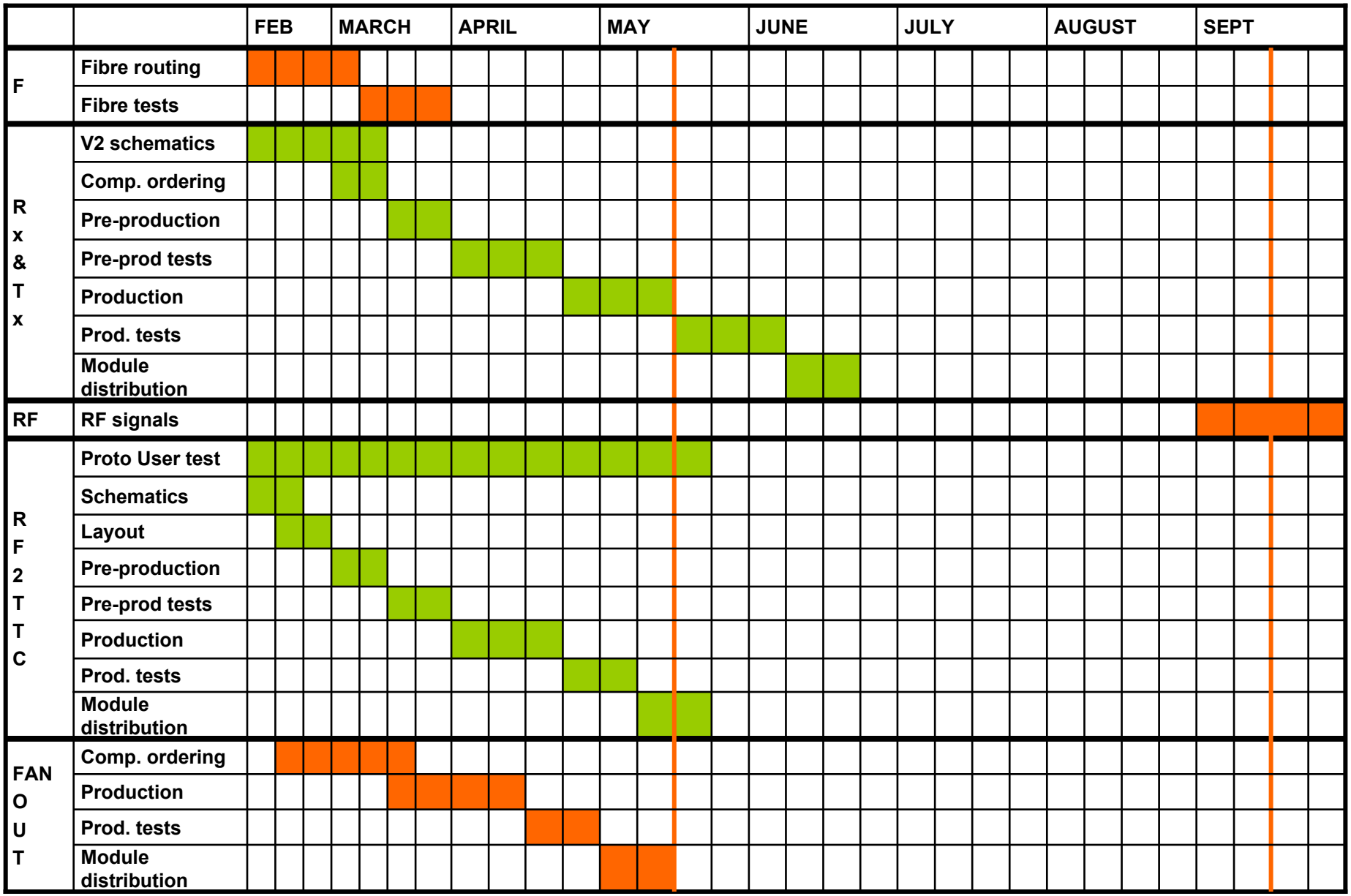
TOTAL (4 exp + support)	Used	Spares	Unit Price	Total Price
Fibres, patches			?	?
Crate (bin, fantray, power supply)			0	0
Crate controller			0	0
RF_Tx	4	4 [2]	3.5	28 [21]
RF_Rx	10	10 [5]	2.5	50 [37.5]
RF2TTC	5	10 [5]	2.5	37.5 [25]
Fanout	5	5 [3]	2.5	25 [20]
				140.5 [103]

Price per exp : **35 kCHF [26 kCHF]**

Financial contribution will be asked during 2007

Estimated price in November 2005: 40 kCHF/exp

FULL SYSTEM [schedules]



FULL SYSTEM [maintenance & support]

	First tests (module exchange with a spare if available)	Piquet	Support (working hours technical help)	Maintenance
Crate (bin, fantray, power supply)	Exp		PH/ESS	POOL
Crate controller	Exp		PH/ESS	POOL
Transmission quality	AB/RF	AB/RF		
RF_Rx	Exp	AB/RF	AB/RF, PH/ESS	PH/ESS
RF2TTC	Exp		PH/ESS	PH/ESS
Fanout	Exp		PH/ESS	PH/ESS
Special components (6dB attenuators, SMA to Lemo adaptors)			PH/ESS (paying service)	

FULL SYSTEM [summer plans]

- I will be away from mid-May until mid-September
- Stephane DETRAZ will take care of the support, maintenance and help to installation during this time
  - TTC general support
  - RF_Rx reception and distribution to users
    - Ageing cycles
  - Technical help for the setup of the TTC upgrade system

- System overview
- Optical Tx and Rx modules
- RF2TTC module
- Fanout
- TTC Crate
- Full system
- Documentation
- AOB

DOCUMENTATION

Project web page:

http://ttc-upgrade.web.cern.ch/ttc-upgrade/Default.htm

System test report:

http://ttc-upgrade.web.cern.ch/ttc-upgrade/New_system/TTCupgrade_System_Test_report.pdf

RF_Rx (&Tx):

The following information is available from the web site:

http://ttc-upgrade.web.cern.ch/ttc-upgrade/New_system/RF_Rx_D.htm

- OCP-STX and SRX modules datasheet
- TRR-1B43-000 datasheet
- First evaluation of the SDH/SONET and TRR transmitters and receivers
- Final test of the Version1 modules
- EDMS Schematics and Layout of the RF_Tx_D: EDA-01380
- EDMS Schematics and Layout of the RF_Rx_D: EDA-01382
- RF_Tx_D User Manual
- RF_Rx_D User_Manual
- CVS repository for RF_Tx_D and RF_Rx_D graphical control panels (tcl&tk panels)
- Money spent for the RF_Tx_D and for the RF_Rx_D:

RF2TTC:

The following information is available from the web site:

http://ttc-upgrade.web.cern.ch/ttc-upgrade/New_system/RF2TTC.htm

- Design Review: TTC project page on the Indico Server
- RF2TTC User Manual - last submission: 30/01/2007
- RF2TTC test results
- Schematics and Layout of the RF2TTC: EDA-01357
- CVS repository for RF2TTC control software
- Analysis of the board layout with SpecctraQuest, made by Alexandra Dana Oltean Karlsson, to understand the differences between the BCref and the other Clock paths (40ps rms jitter instead of 26): board analysis, vias extraction
- VHDL code of the FPGA.
- Money spent of the RF2TTC

- System overview
- Optical Tx and Rx modules
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AOB

- AB/RF and PH/ESS joined presentation about timing probably at LEADE end of April
- TTCex new batch – anybody interested?
  - Opportunity to put some of these modules at the pool…. Interested?